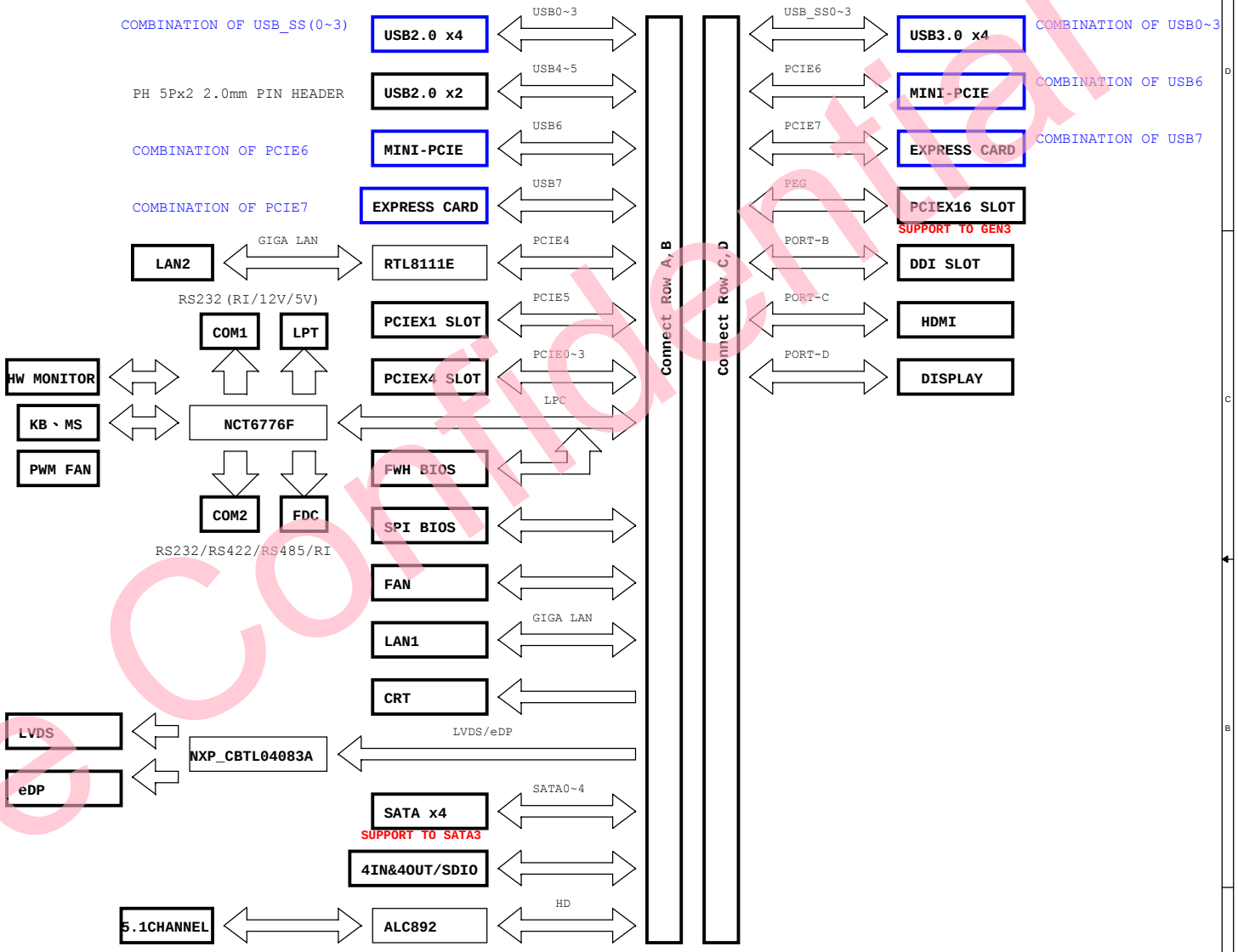
BLOCK DIAGRAM



PCB p/n : E1907EX1405RO A2

PCB1

EEV-EX14-A2/PCB/6L

文字標示:
EEV-EX14 A2
E1907EX1405RO-W1
MADE IN TAIWAN

LAYOUT NOTE:紅色字 或 紅色框 或 CLOSE TO... 或 LAYOUT...

電阻部份
1.0402不標示
2.5%不標示
3.1%及非0402要做標示
如10KR06/1%

電容部份
1.0402不標示,但10uF全為0805也不標
2.10uF(0805)及0.1uF(0402)的16V也不標
3.0.1uF少數耐壓50V的,均用0603,均需做標示
4.電容均用X5R X7R 除耐大電壓之電容
5.其他uF pF電壓值不標示,因均大於16V

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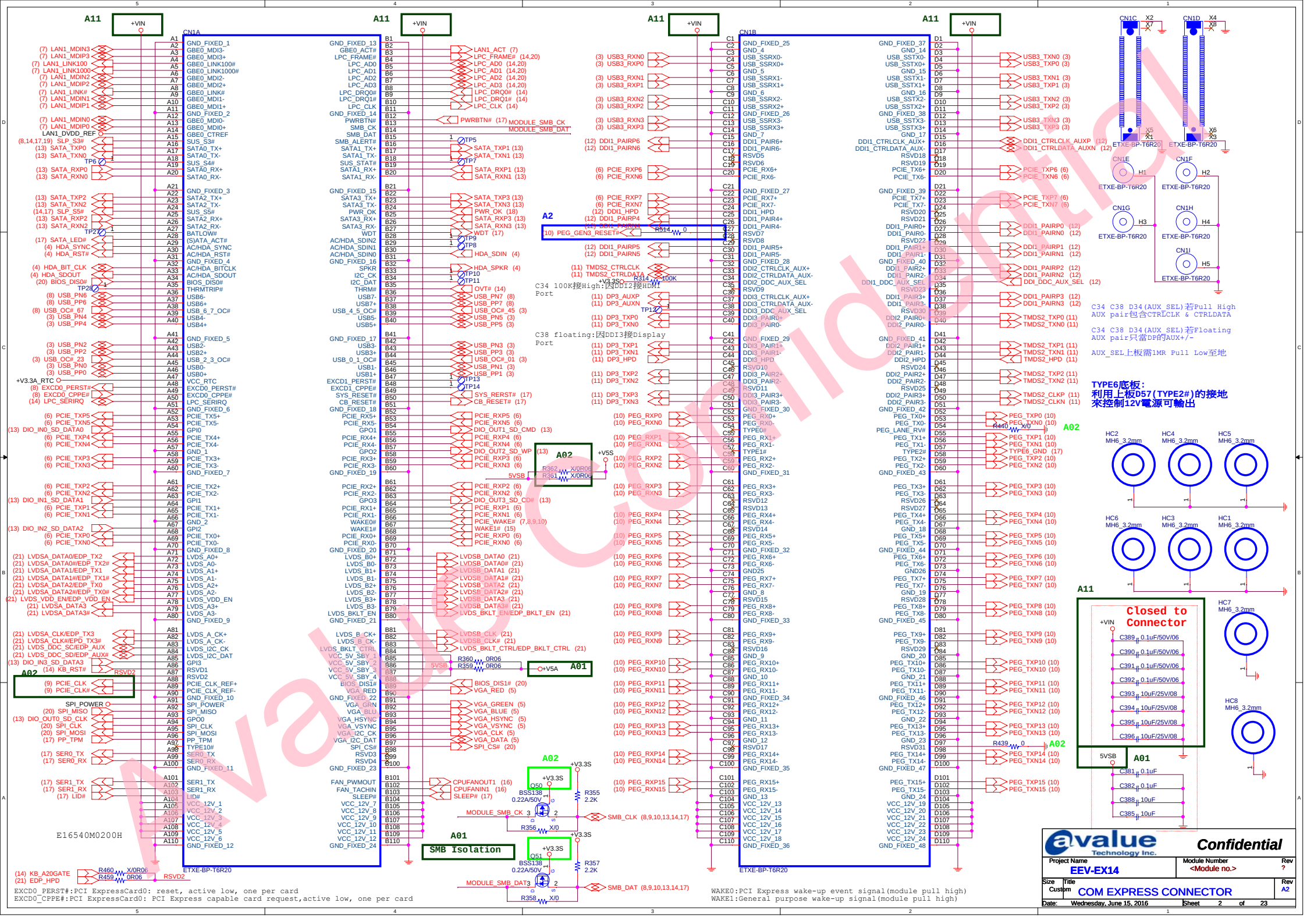
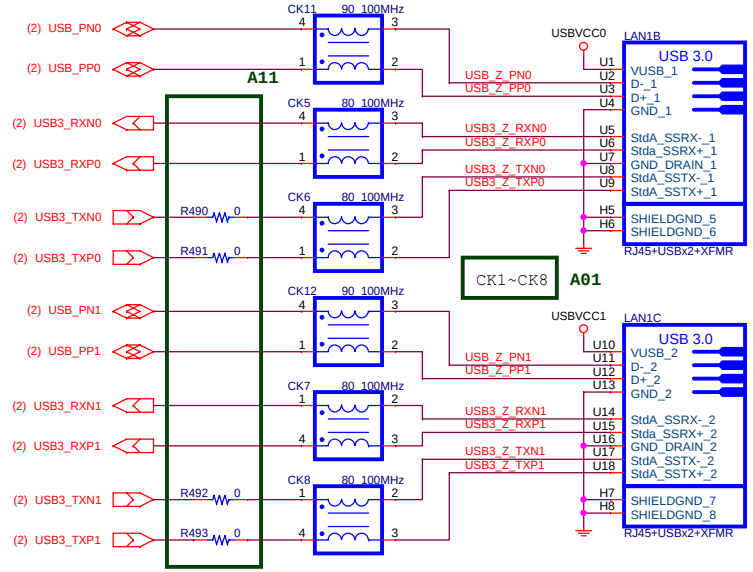
Project Name	Module Number	Rev
EEV-EX14	<Module no.>	?

Size	Title	Rev
A3	BLOCK DIAGRAM	A2

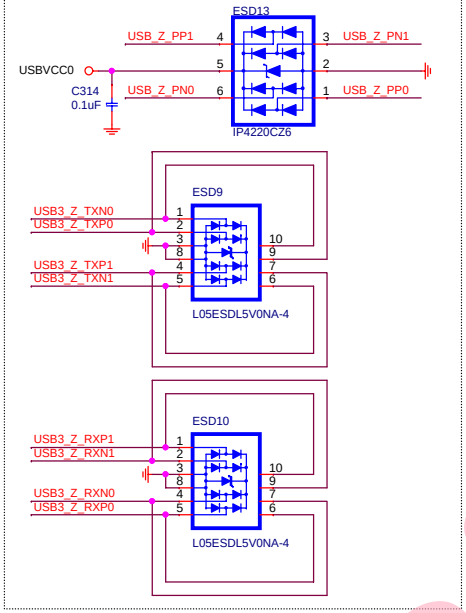
Date: Wednesday, June 15, 2016 Sheet 1 of 23


A11
+VIN
CN1A
ETXE-BP-T6R20
A02
A01
SMB Isolation
CN1B
CN1C
CN1D
CN1E
CN1F
CN1G
CN1H
CN1I
Closed to Connector
C34 C38 D34(AUX_SEL)若Pull High AUX pair包含CTRCLK & CTRLDATA
C34 C38 D34(AUX_SEL)若Floating AUX pair只當DP的AUX+/-
AUX_SEL上板需1MR Pull Low至地
TYPE6底板：利用上板D57(TYPE2#)的接地來控制12V電源可輸出
C34 100K接High:因DDI2接HDMI Port
C38 floating:因DDI3接Display Port
EXCD0_PERST#:PCI ExpressCard0: reset, active low, one per card
EXCD0_CPPE#:PCI ExpressCard0: PCI Express capable card request,active low, one per card
WAKE0:PCI Express wake-up event signal(module pull high)
WAKE1:General purpose wake-up signal(module pull high)
E16540M0200H
Confidential
Project Name
EEV-EX14
Module Number
<Module no.>
Title
COM EXPRESS CONNECTOR
Size
Custom
Date:
Wednesday, June 15, 2016
Sheet
2
of
23

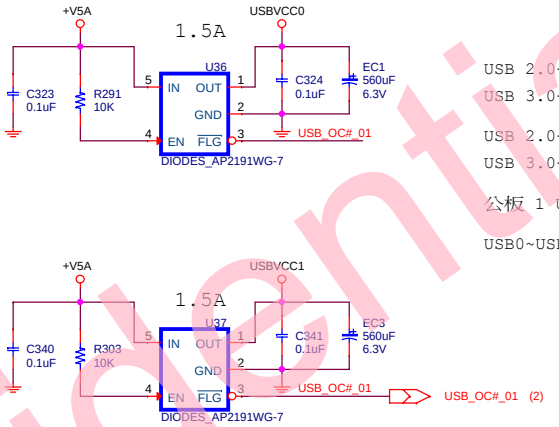
USB0 and USB1(USB2.0+USB3.0)



Closed to Connector



OC Pull High於上板



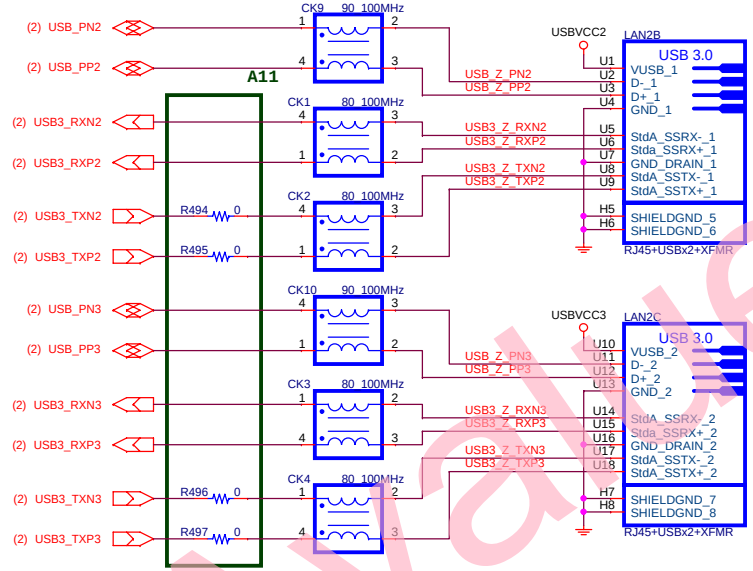
USB 2.0-->480Mbps(bit width 2083ps)
USB 3.0-->5Gbps(bit width 200ps)

USB 2.0-->5x100mA=0.5A
USB 3.0-->6x150mA=0.9A

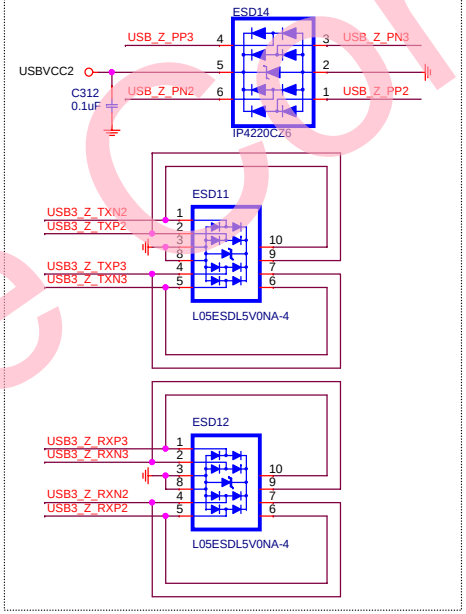
公板 1 USB port 放220uF

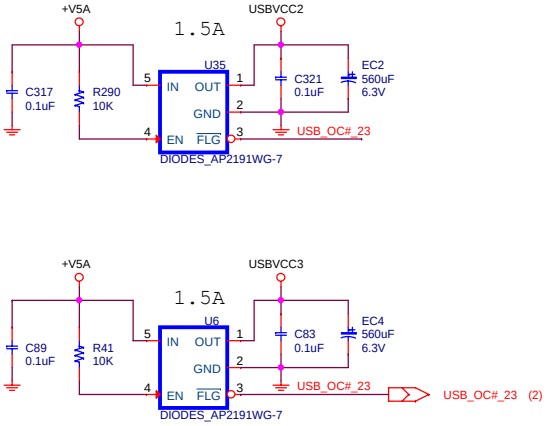
USB0~USB3 MAX 1.5A/Port

USB2 and USB3(USB2.0+USB3.0)

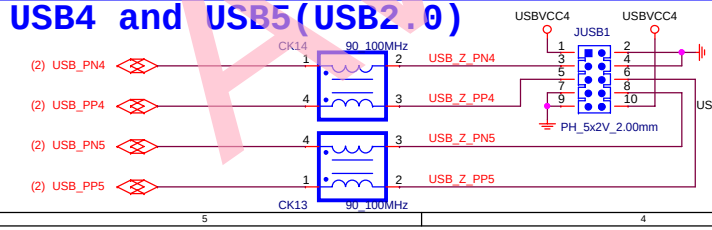


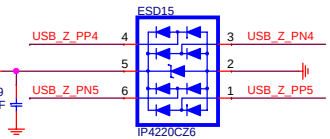
Closed to Connector

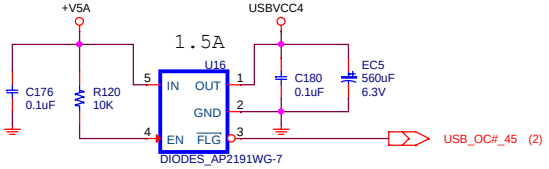




USB4 and USB5(USB2.0)







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Project Name	Module Number	Rev
EEV-EX14	IO-04	A0

Size	Title	Rev
A3	USB2.0(0-5)、USB3.0(0-3)	A2

Date: Wednesday, June 15, 2016 Sheet 3 of 23

HD Audio(ALC892)

```
Sense:
PortA(39,41):SenseA,39.2K
PortB(21,22):SenseA,20K
PortC(23,24):SenseA,10K
PortD(35,36):SenseA,5.1K
PortE(14,15):SenseB,39.2K
PortF(16,17):SenseB,20K
PortG(43,44):SenseB,10K
PortH(45,46):SenseB,5.1K
```

ALC892用不到PIN37&33,故永不用接

Closed to IC

PIN25/28為ALC892內部LDO Output
接在一起並各放X5R 10u and 0.1u電容

Closed to IC

Analog

Digital

+V5S 0.046A

+V3.3S 0.012A

Closed to IC

Analog

Digital

A01

A01

特定南橋要求使用(如GM45)
當要使用HDMI HD Audio時
HDA_xxx準位要為1.5V
PIN10則需改接1.5V

S/PDIF

BUZZER

CD_IN

Use 1K-Ohm may enhance audio ESDprotection

For HDA/AC97 front panel

PORT E

PORT F

*Intel Define:Pin8 NC
Realtek Define:Pin6 NC

Intel Define:Pin7 to Codec,Pin6 link R to GND
*Realtek Define:Pin7 to GND,Pin6 link R to Codec

PORT C

Use 1K-ohm for dedicated input function may enhance ESD protection

PORT D

Use 75 Ohm for output function may enhance audio quality and ESD protection

PORT B

MIC1、LINE1 do not support Re-Tasking

PORT G

PORT H

PORT A

此 2 Connector有做小板可測試

加上FRONT_OUT構成7.1聲道

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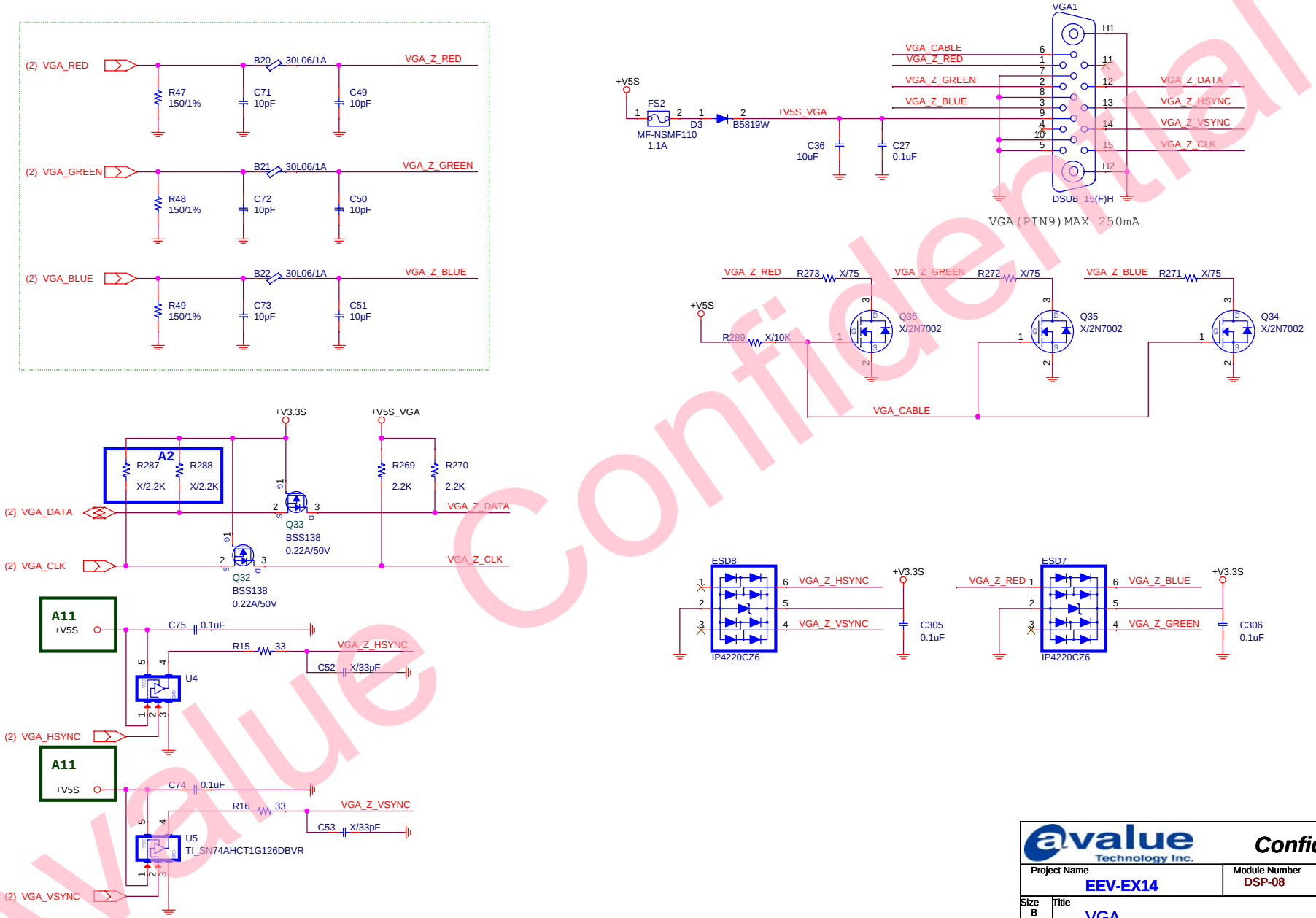
Project Name: EEV-EX14	Module Number: AUD-01	Rev: A01	
Size: A3	Title: AUDIO(ALC892)	Rev: A2	
Date: Wednesday, June 15, 2016	Sheet 4 of 23		



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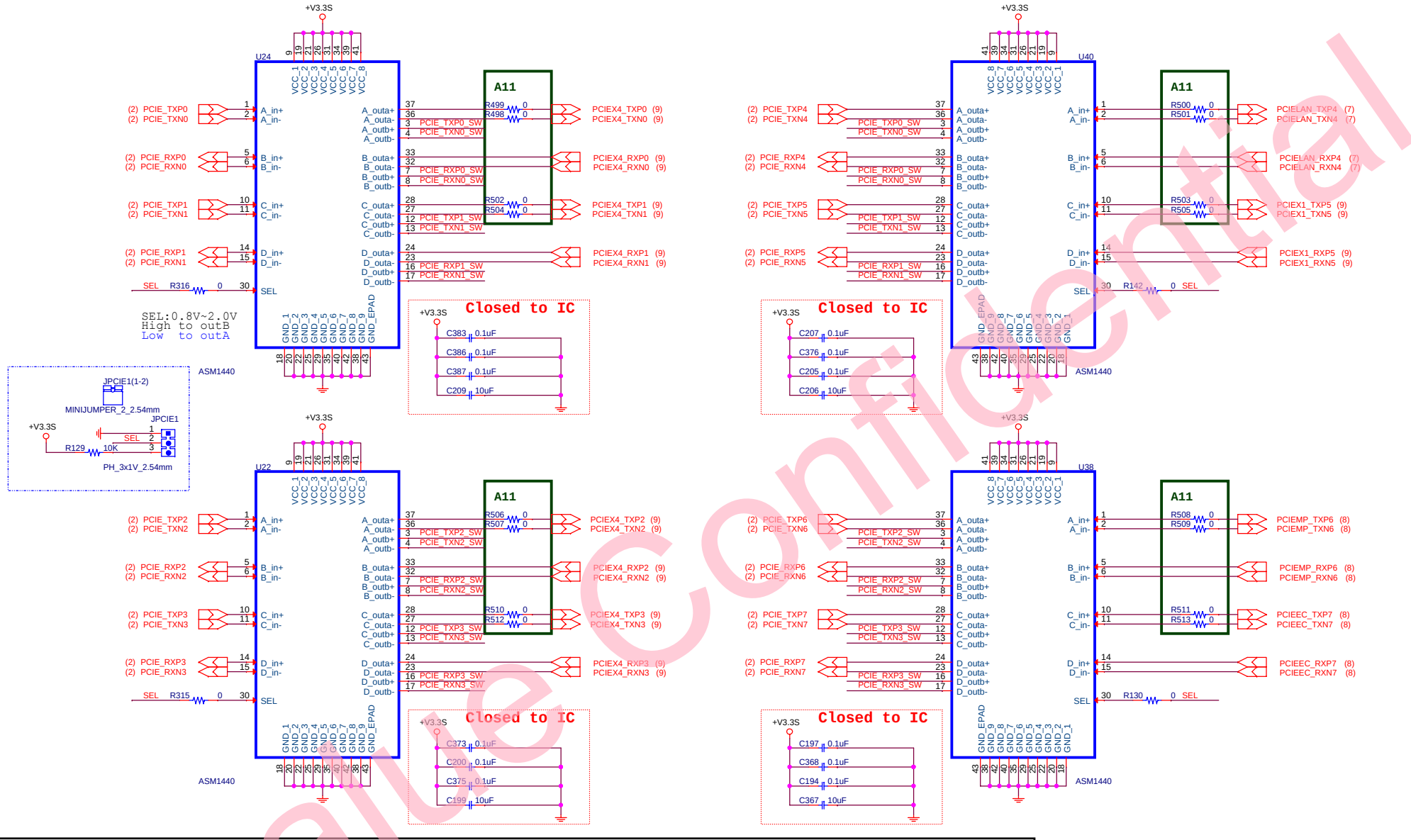
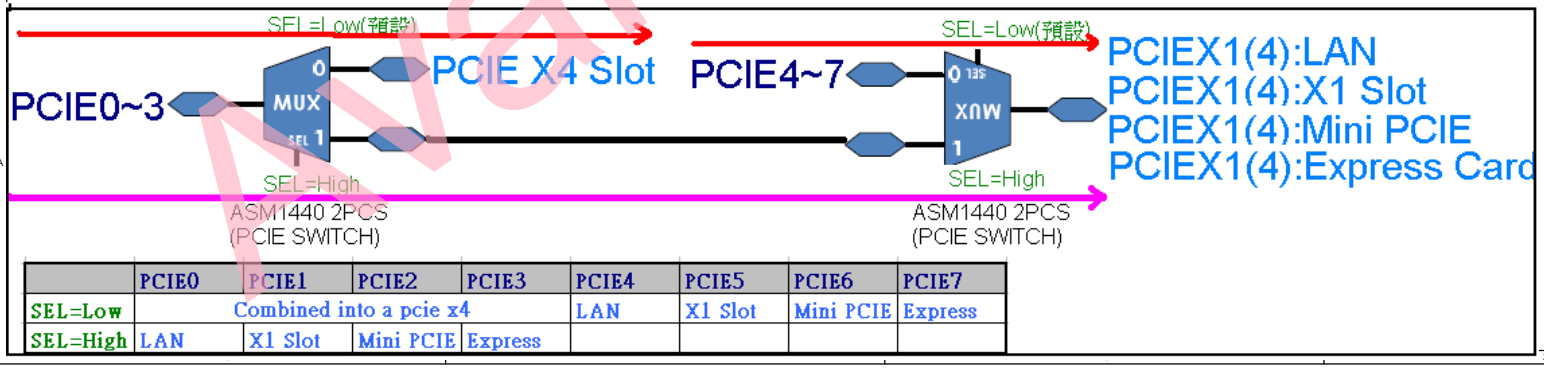
Project Name: EEV-EX14	Module Number: DSP-08	Rev: A01
Size: B	Title: VGA	Rev: A2
Date: Wednesday, June 15, 2016	Sheet 5 of 23	





	PCIE0	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6	PCIE7
SEL=Low	Combined into a pcie x4				LAN	X1 Slot	Mini PCIE	Express
SEL=High	LAN	X1 Slot	Mini PCIE	Express				

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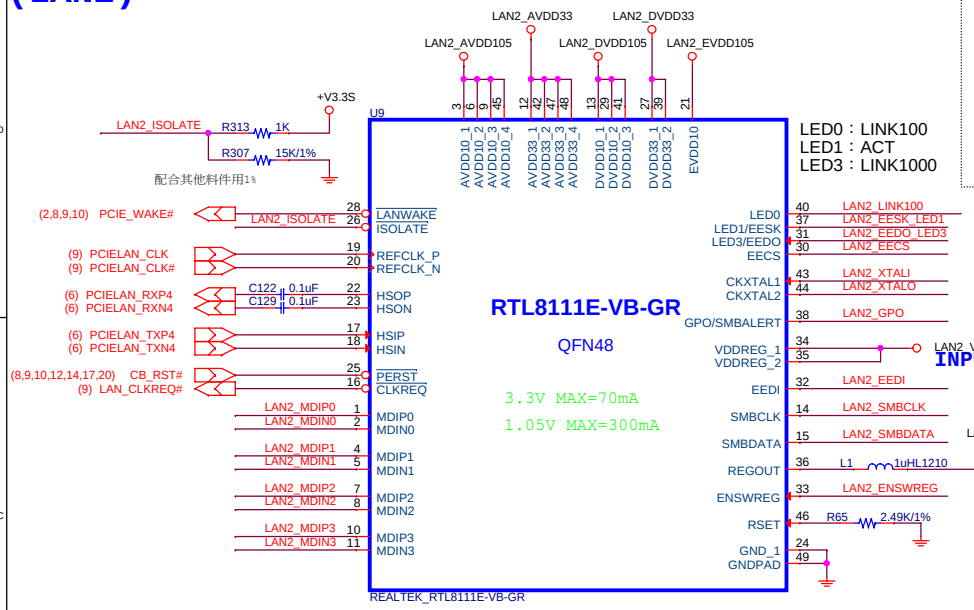
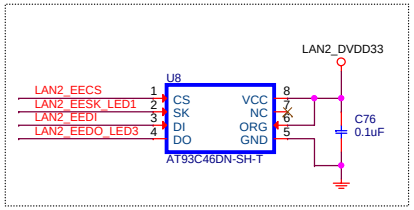
Project Name	Module Number	Rev
EEV-EX14	<Module no.>	?

Size	Title	Rev
A3	PCIE SWITCH	A2

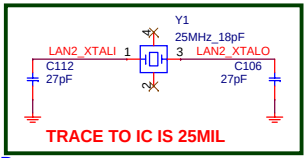
Date: Wednesday, June 15, 2016 Sheet 6 of 23

Carrier Board LAN IC (LAN2)





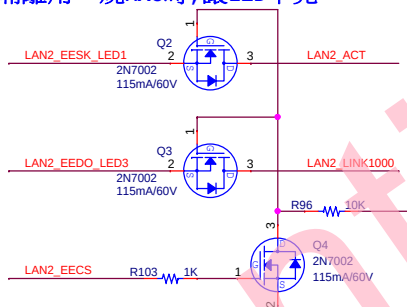
A01



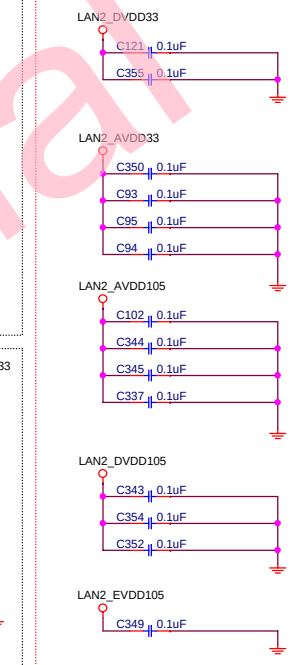
INPUT POWER

OUTPUT POWER

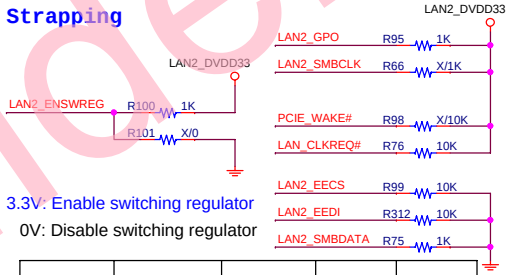
隔離用：燒MAC時，讓LED不亮



Closed to IC



Strapping

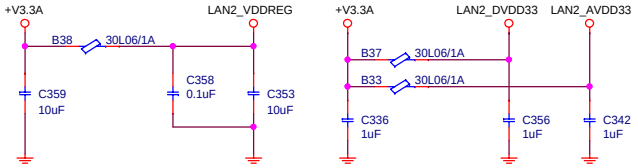


3.3V: Enable switching regulator

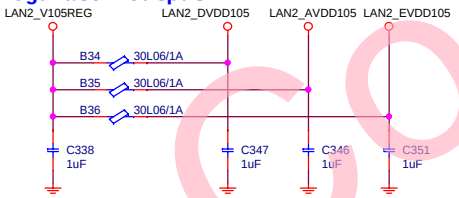
0V: Disable switching regulator

pin number	net name	Function	0	1
15	SMBDATA	ROM size	46	56 / 66
32	EEDI	TWSI/ROM	EEPROM	TWSI
33	LAN1_ENSR	Internal regualtor	Disable	Enable

For Regulater Input



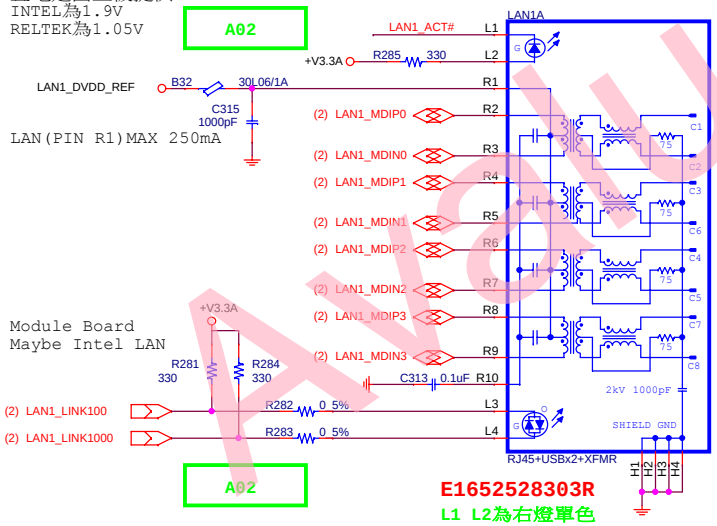
Regulater output



LAN1 Connector

給不給電 由上板LAN CHIP 決定
且電是由上板提供
INTEL為1.9V
RELTEK為1.05V

A02



A02

E1652528303R

L1 L2為右燈單色

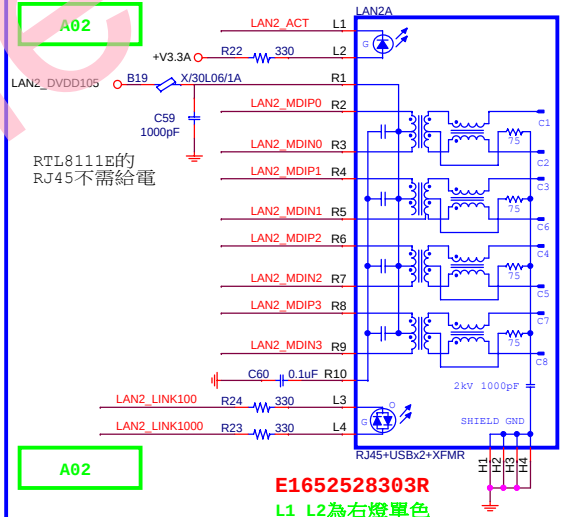
LAN2 Connector

LAN1~LAN2

A01

RTL8111E LED0、3需為1組
不需另外Pull High(L3、L4)

A02



A02

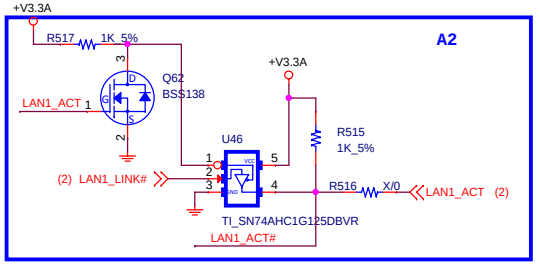
E1652528303R

L1 L2為右燈單色

LAN LED Active

LAN2 Connector

	single LED	Dual LED	
	(green)	(green)	(orange)
10M	Blinking	X	X
100M	always ON	always ON	X
1000M	always ON	X	always ON



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Project Name	Module Number	Rev
EEV-EX14	LAN-03	A0

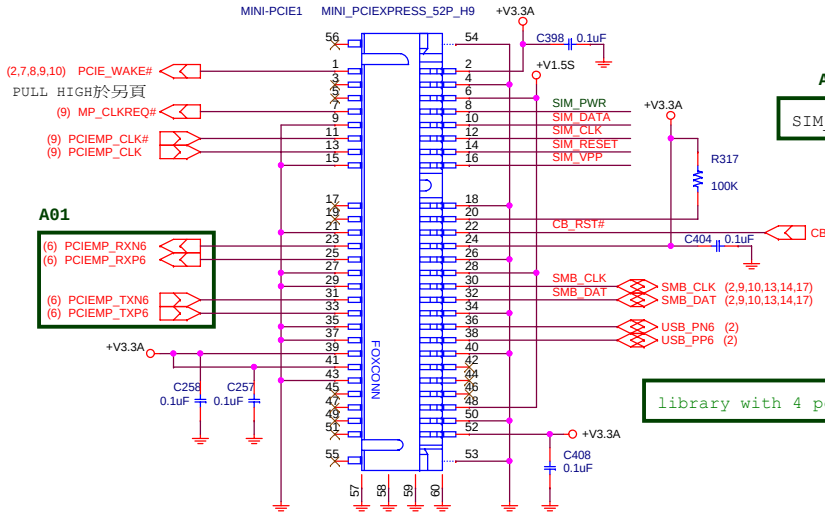
Size	Title	Rev
A3	LAN1、LAN2(RTL8111E)	A2

Date: Wednesday, June 15, 2016 Sheet 7 of 23

Mini_PCIE SLOT

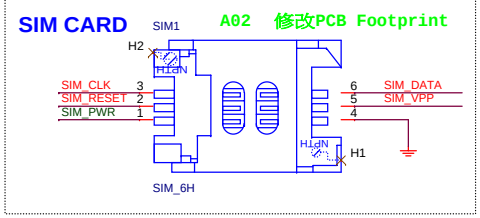
PCB Footprint已改成非CIS
CIS有此料號，但未含4個桐柱的孔
故請layout修改完後另存成新的PCB Footprint
E1654252133R為H9.0高Connector

SIM library 有偏，有再做調整成SIM_6P_254016MA006G100ZL_D



A01
SIM_PWR

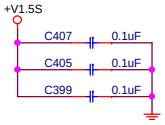
SIM CARD



MPCIE1#1 SCREW
MPCIE1#2 SCREW
無CIS

library with 4 pcs Screw holes(#1~#4)

Closed to MPCIE1



Mini PCI-E

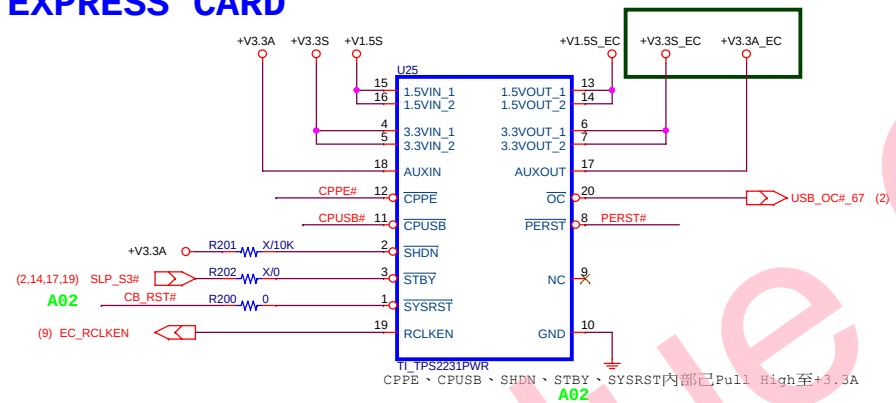
Pin	Ver1.0	Ver1.2	Pin	Ver1.0	Ver1.2
1	WAKE#	WAKE#	2	+3.3V	+3.3Vaux
3	COEX1	COEX1	4	GND	GND
5	COEX2	COEX2	6	+1.5V	+1.5V
7	CLKREQ#	CLKREQ#	8	UIM_PWR	UIM_PWR
9	GND	GND	10	UIM_DATA	UIM_DATA
11	REFCLK-	REFCLK-	12	UIM_CLK	UIM_CLK
13	REFCLK+	REFCLK+	14	UIM_RESET	UIM_RESET
15	GND	GND	16	UIM_VPP	UIM_VPP
Mechanical Key					
17	UIM_C8	UIM_C8	18	GND	GND
19	UIM_C4	UIM_C4	20	W_DISABLE#	W_DISABLE#
21	GND	GND	22	PERST#	PERST#
23	PERn0	PERn0	24	+3.3Vaux	+3.3Vaux
25	PERp0	PERp0	26	GND	GND
27	GND	GND	28	+1.5V	+1.5V
29	GND	GND	30	SMB_LCK	SMB_LCK
31	PETn0	PETn0	32	SMB_DATA	SMB_DATA
33	PETp0	PETp0	34	GND	GND
35	GND	GND	36	USB_D-	USB_D-
37	Reserved	GND	38	USB_D+	USB_D+
39	Reserved	+3.3Vaux	40	GND	GND
41	Reserved	+3.3Vaux	42	LED_WWAN#	LED_WWAN#
43	Reserved	GND	44	LED_WLAN#	LED_WLAN#
45	Reserved	Reserved	46	LED_WPAN#	LED_WPAN#
47	Reserved	Reserved	48	+1.5V	+1.5V
49	Reserved	Reserved	50	GND	GND
51	Reserved	Reserved	52	+3.3V	+3.3Vaux

Mini PCI-E Ver 1.2 Power

Power	Voltage	Primary Power		Auxiliary Power
		Peak mA	Normal mA	Normal mA
+3.3Vaux	±9%	2750	1100	250(wake EN)
+1.5V	±5%	500	375	N/A
+1.5V	±5%	500	375	N/A

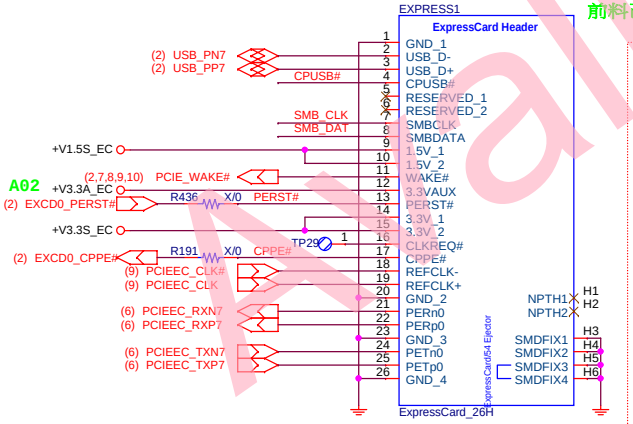
EXPRESS CARD

A01

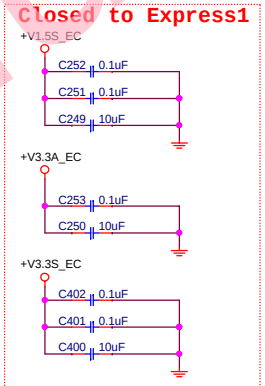


CPPE、CPUSB、SHDN、STBY、SYSRST內部已Pull High至+3.3A

A02 前料已停產 換新料 無CIS



Closed to Express1

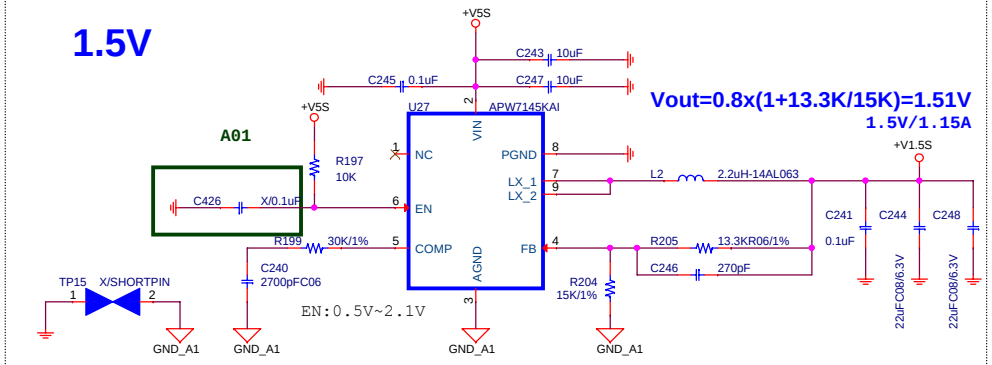


A02 前料已停產 換新料 無CIS

EXPRESS2
ExpressCard/54 Ejector
ExpressCard/54_EJECTOR

EXPRESS1#1 SCREW
EXPRESS1#2 SCREW

1.5V



Vout=0.8x(1+13.3K/15K)=1.51V
1.5V/1.15A

Supply	Limits[2]
+3.3V[1]	1000 mA – Average 1300 mA – Max
+3.3VAUX[1]	250 mA – Average 275 mA – Max
	5 mA – Average
+1.5V	500 mA – Average 650 mA – Max

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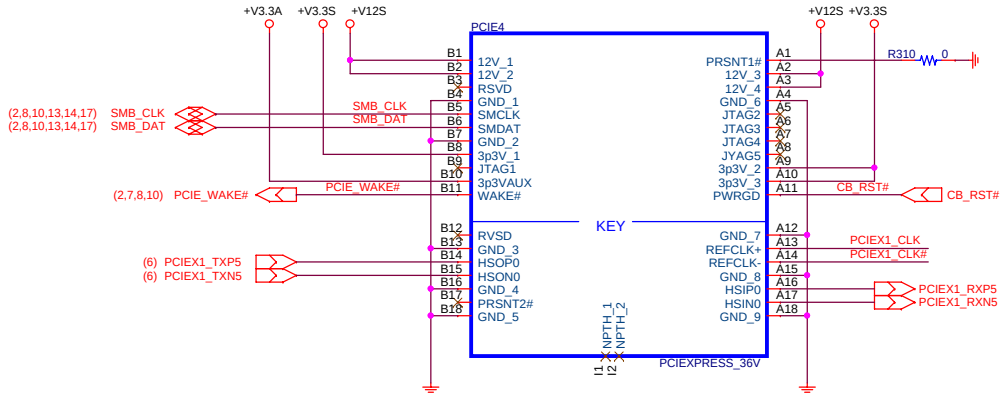
Project Name	Module Number	Rev
EEV-EX14	SLT-04	A1

Size	Title	Rev
A3	MINI PCIE CARD、EXPRESS CARD	A2

Date: Wednesday, June 15, 2016 Sheet 8 of 23

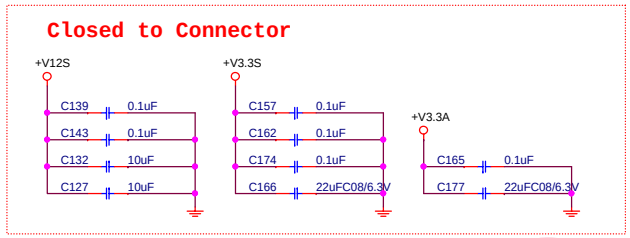
PCIE X1 SLOT



参考COM Expree Datasheet
X1 JTAG ALL NC
PIN B3: Only PCIE X4 X16 Link 12V
PIN A11: Define PERST#

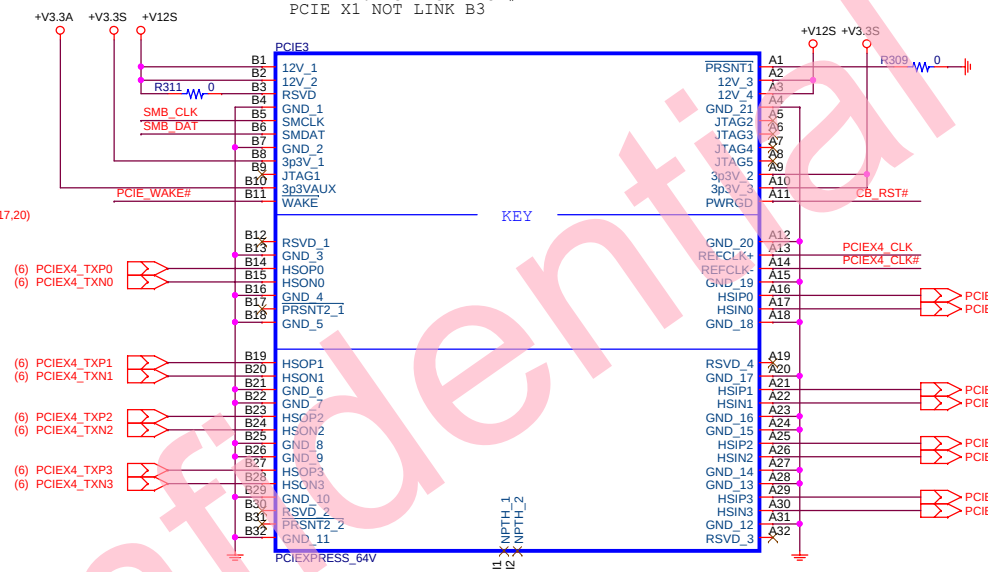
PIN A1、B17用法:支援電源熱插拔用

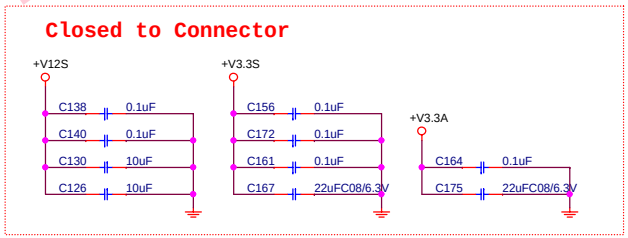
A1 接GND,B17 Pull High,
CARD Device會將此2pin相連,
故底板B17就可控制電源輸出或通知BIOS

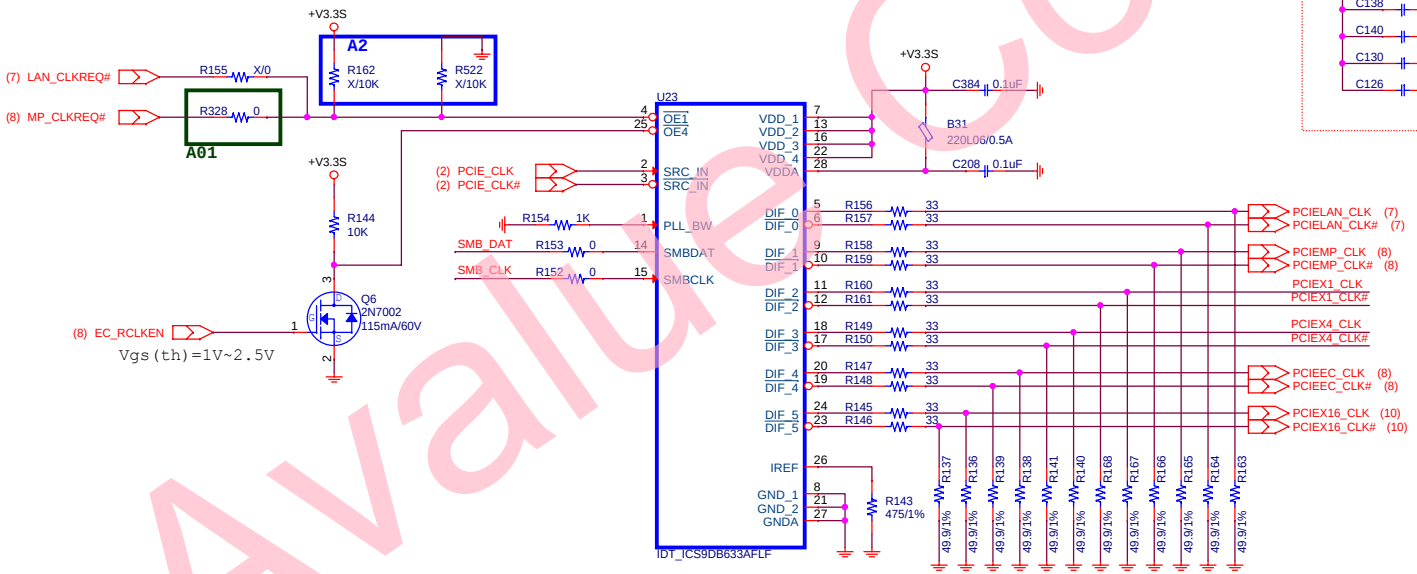


PCIE X4 SLOT

參考COM Expree Datasheet
X4 JTAG ALL NC
PIN B3: Only PCIE X4 X16 Link 12V
PIN A11: Define PERST#
PCIE X1 NOT LINK B3







33及49.9均不需用1%

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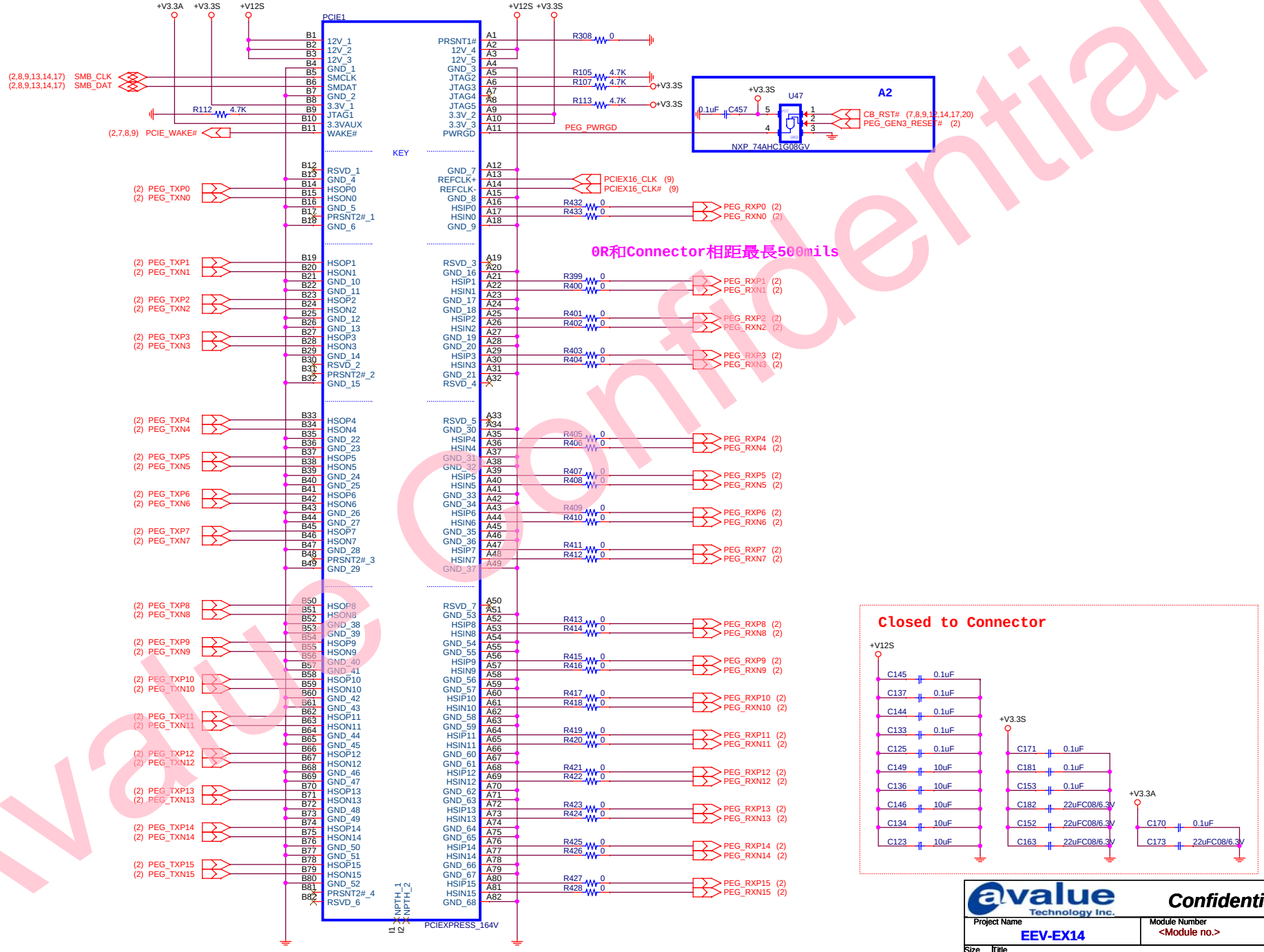
Project Name: EEV-EX14	Module Number: <Module no.>	Rev: ?
Size: A3	Title: PCIEX1、PCIEX4、CLOCK BUFFER	Rev: A2
Date: Wednesday, June 15, 2016	Sheet 9 of 23	

参考COM Expree Datasheet
X16 JTAG 接法如下
PIN B3: Only PCIE X4 X16 Link 12V
PIN A11: Define PERST#



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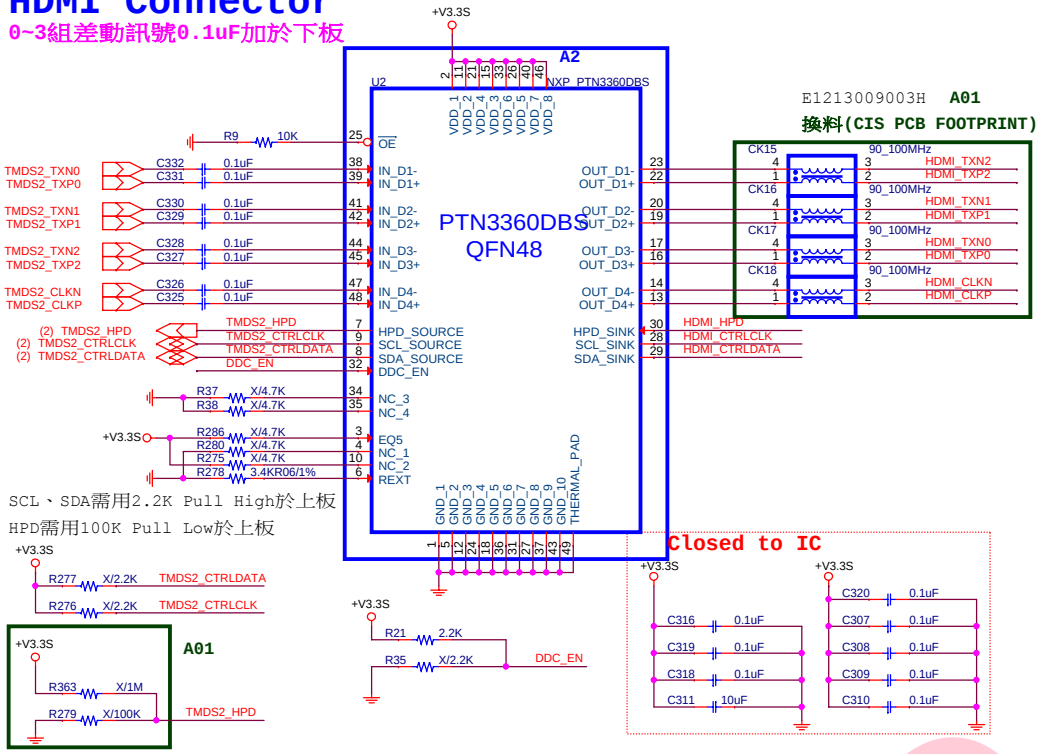
Project Name: EEV-EX14		Module Number: <Module no.>	Rev: ?
Size: A3	Title: PCIEX16		Rev: A2
Date: Wednesday, June 15, 2016		Sheet 10 of 23	

HDMI Connector

0~3組差動訊號0.1uF加於下板

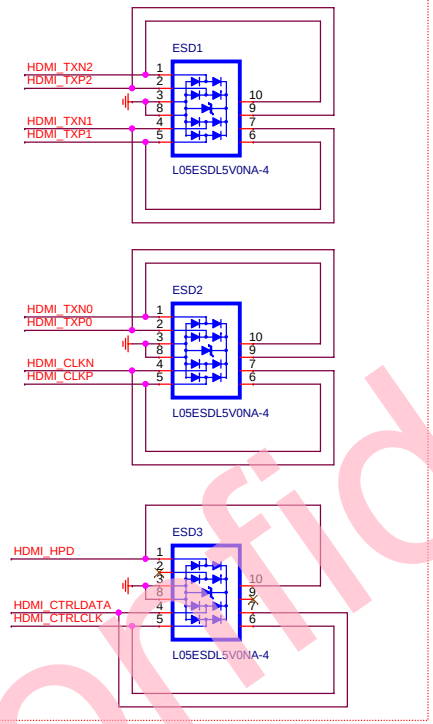


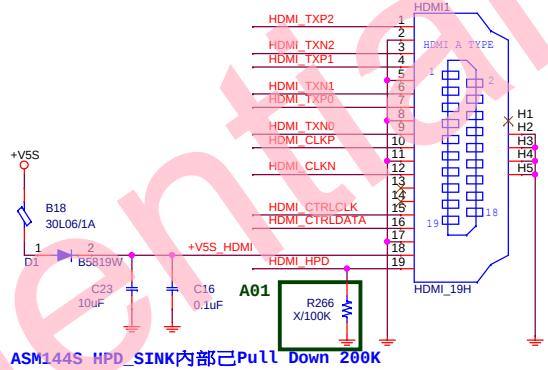
E1213009003H A01

換料(CIS PCB FOOTPRINT)

Closed to IC

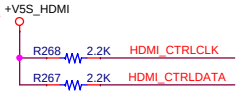
Closed to Connector

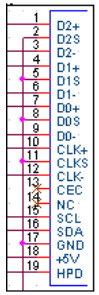




ASM144S HPD_SINK內部已Pull Down 200K

HDMI(PIN18)MAX 50mA

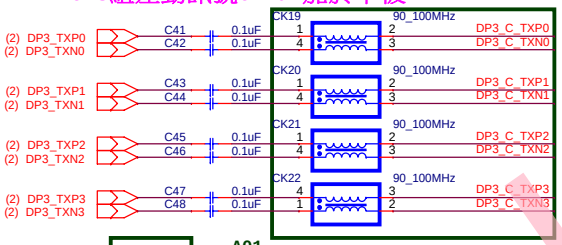




Display Connector

0~3組差動訊號0.1uF加於下板

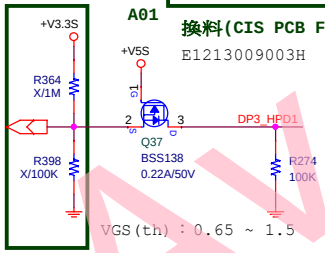
A01



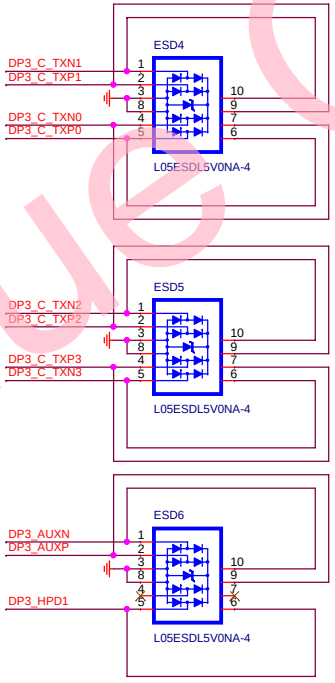
A01

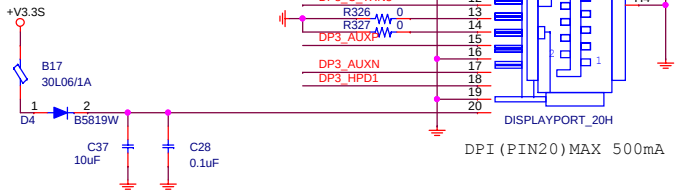
換料(CIS PCB FOOTPRINT)

E1213009003H



Closed to Connector





DPI(PIN20)MAX 500mA

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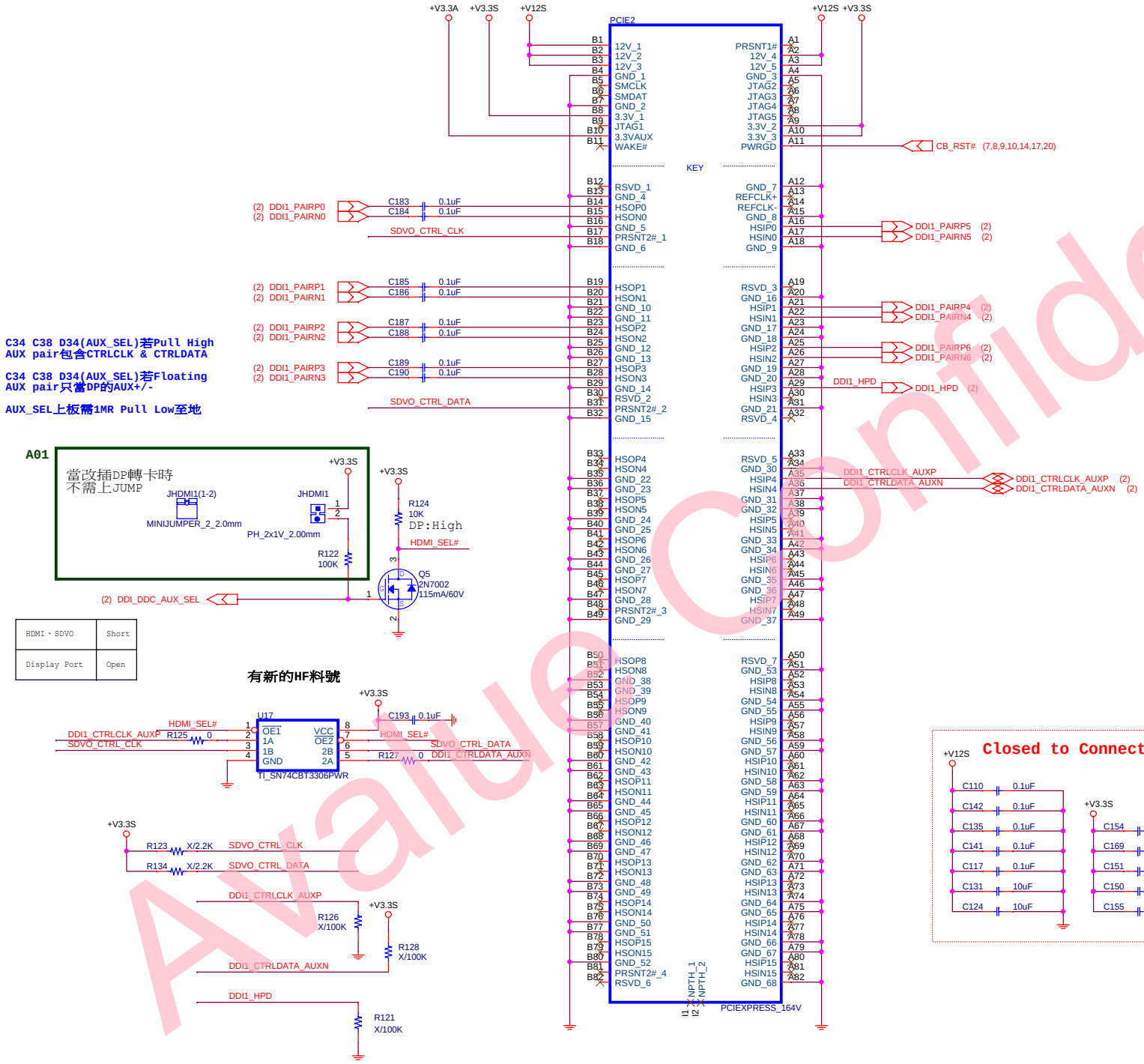
Project Name: EEV-EX14		Module Number: <Module no.>	Rev: ?
Size: A3	Title: HDMI、DISPLAY		Rev: A2
Date: Wednesday, June 15, 2016		Sheet 11 of 23	

ADD2N CARD SLOT

料號改過：藍色SLOT



C34 C38 D34(AUX_SEL)若Pull High
AUX pair包含CTRLCLK & CTRLDATA

C34 C38 D34(AUX_SEL)若Floating
AUX pair只當DP的AUX+/-

AUX_SEL上板需1MR Pull Low至地

Pin Name	Type & Pin Number	SDVO	DP	HDMI/DVI (TMDS Signaling)
DDI1_PAIR0+	D26	SDVO1_RED+	DP1_LANE0+	TMDS1_DATA2+
DDI1_PAIR0-	D27	SDVO1_RED-	DP1_LANE0-	TMDS1_DATA2-
DDI1_PAIR1+	D29	SDVO1_GRN+	DP1_LANE1+	TMDS1_DATA1+
DDI1_PAIR1-	D30	SDVO1_GRN-	DP1_LANE1-	TMDS1_DATA1-
DDI1_PAIR2+	D32	SDVO1_BLU+	DP1_LANE2+	TMDS1_DATA0+
DDI1_PAIR2-	D33	SDVO1_BLU-	DP1_LANE2-	TMDS1_DATA0-
DDI1_PAIR3+	D36	SDVO1_CK+	DP1_LANE3+	TMDS1_CLK+
DDI1_PAIR3-	D37	SDVO1_CK-	DP1_LANE3-	TMDS1_CLK-
DDI1_PAIR4+	C25	SDVO1_INT+		
DDI1_PAIR4-	C26	SDVO1_INT-		
DDI1_PAIR5+	C29	SDVO1_TVCLKIN+		
DDI1_PAIR5-	C30	SDVO1_TVCLKIN-		
DDI1_PAIR6+	C15	SDVO1_FLDSTALL+		
DDI1_PAIR6-	C16	SDVO1_FLDSTALL-		
DDI1_HPD	C24		DP1_HPD	HDMI1_HPD
DDI1_CTRLCLK_AUX+	D15	SDVO1_CTRLCLK	DP1_AUX+	HMDI1_CTRLCLK
DDI1_CTRLDATA_AUX-	D16	SDVO1_CTRLDATA	DP1_AUX-	HMDI1_CTRLDATA
DDI1_DDC_AUX_SEL	D34			

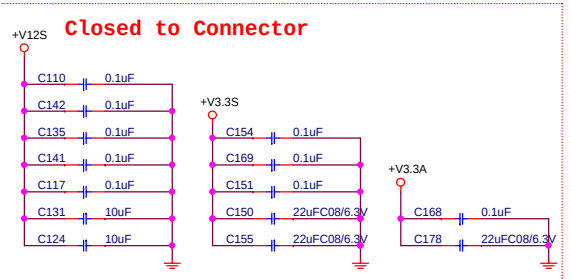
DDI 1

A01

HDMI、SDVO	Short
Display Port	Open

有新的HF料號

Closed to Connector



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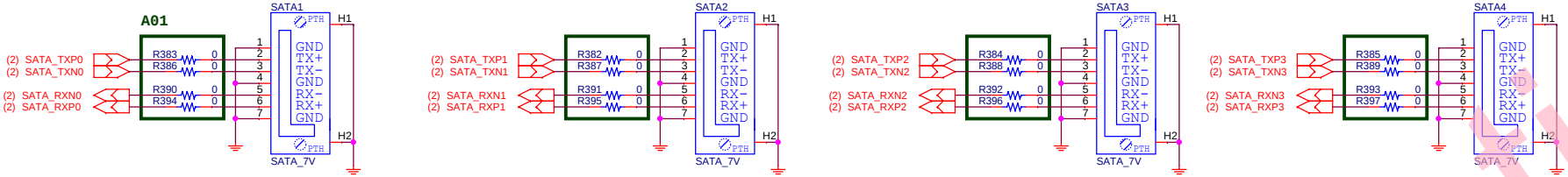
Project Name: EEV-EX14	Module Number: <Module no.>	Rev: ?
Size: A3	Title: DDI SLOT	Rev: A2
Date: Wednesday, June 15, 2016	Sheet 12 of 23	

SATA1~4

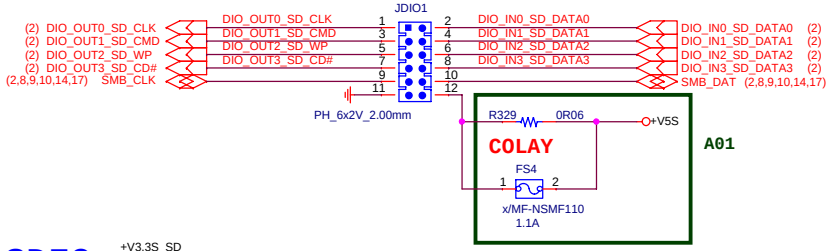
0R和SATA Connector相距最長100mils

TX RX 電容 均應加於上板

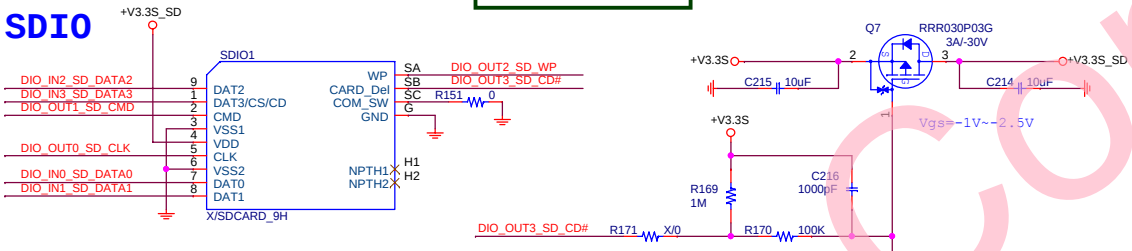


DIO(4IN/4OUT)

上板決定為:DIO功能或SDIO功能



SDIO



COM Express Signal	SD card interface signals
GPI0	SD_DATA0
GPI1	SD_DATA1
GPI2	SD_DATA2
GPI3	SD_DATA3
GPO0	SD_CLK
GPO1	SD_CMD
GPO2	SD_WP
GPO3	SD_CD#

SD_CMD需Pull High於上板

SD_WP 需Pull High於上板

SD_CD#需Pull High於上板

Card detection switch		Write protection switch		
When card is ejected	When card is inserted	When card is ejected	When card is inserted	
			Write protect	Write enable
OPEN	CLOSE	OPEN	OPEN	CLOSE
Sb Sc	Sb Sc	Sa Sc	Sa Sc	Sa Sc

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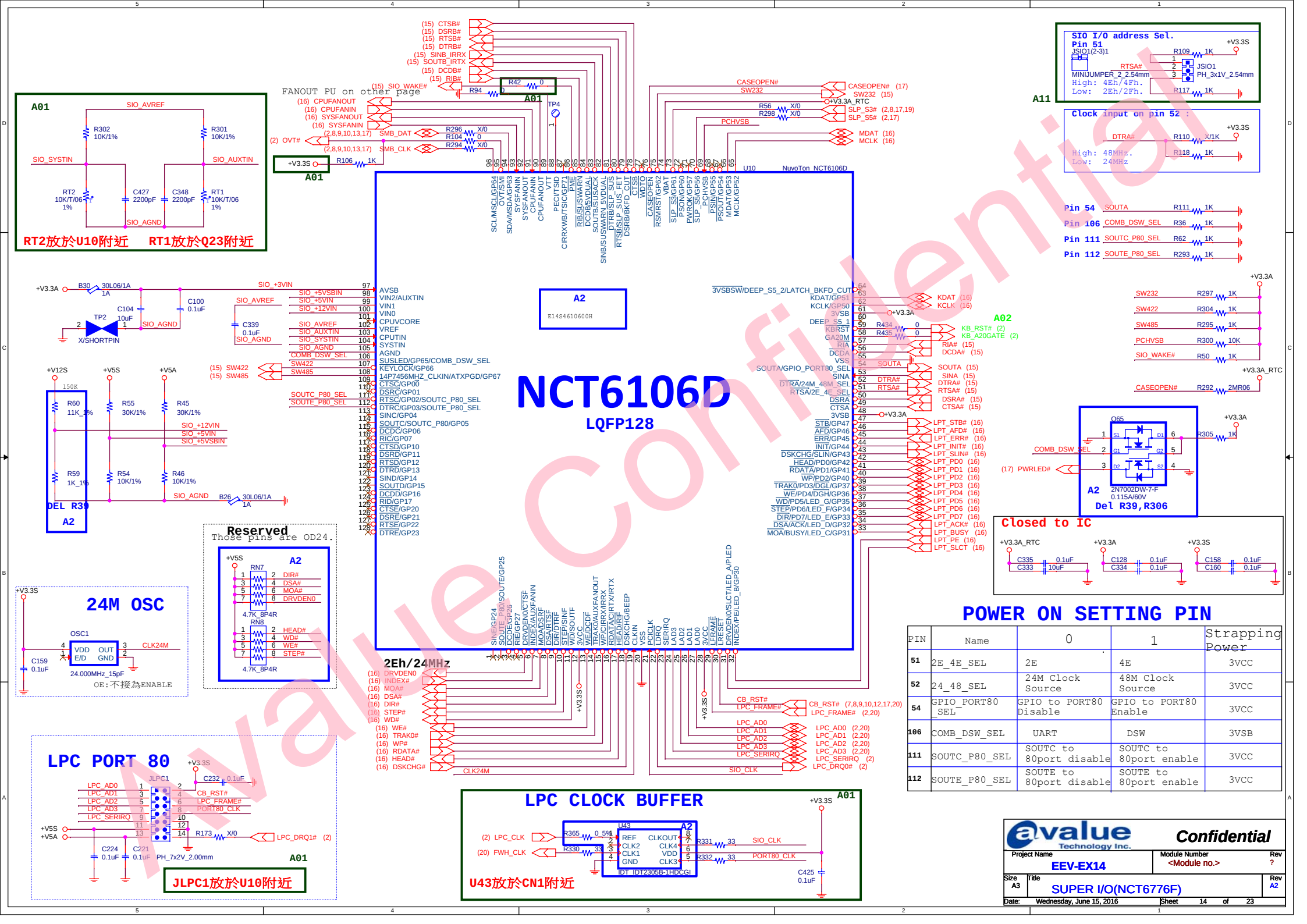
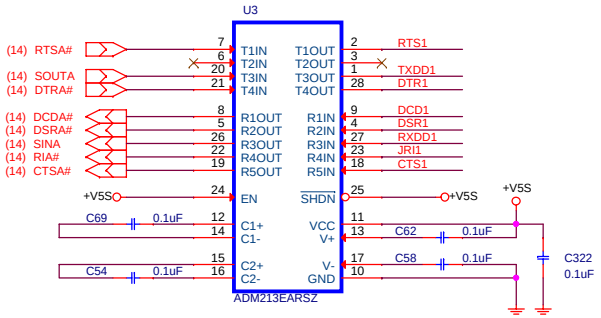
Project Name: EEV-EX14		Module Number: <Module no.>	Rev: ?
Size: A3	Title: SATA、SD、DIO		Rev: A2
Date: Wednesday, June 15, 2016	Sheet 13 of 23		

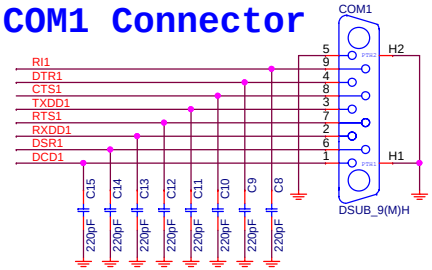


PIN	Name	0	1	Strapping Power
51	2E_4E_SEL	2E	4E	3VCC
52	24_48_SEL	24M Clock Source	48M Clock Source	3VCC
54	GPIO_PORT80 _SEL	GPIO to PORT80 Disable	GPIO to PORT80 Enable	3VCC
106	COMB_DSW_SEL	UART	DSW	3VSB
111	SOUTC_P80_SEL	SOUTC to 80port disable	SOUTC to 80port enable	3VCC
112	SOUTE_P80_SEL	SOUTE to 80port disable	SOUTE to 80port enable	3VCC

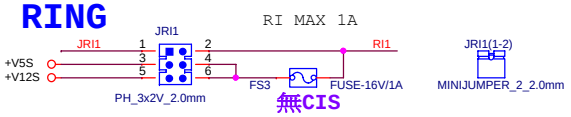
COM1

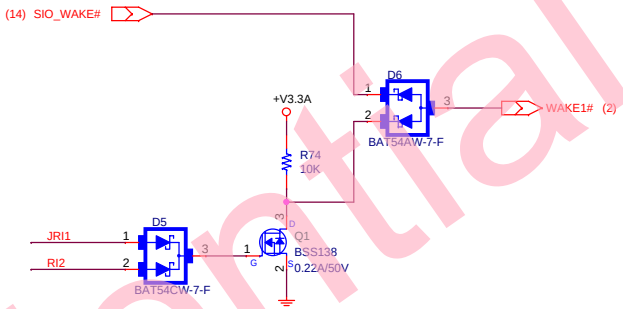


COM1 Connector

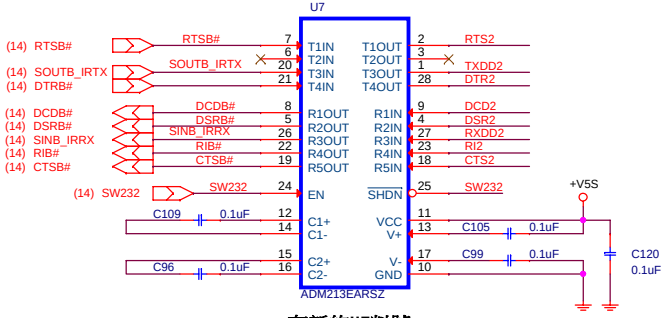


RING

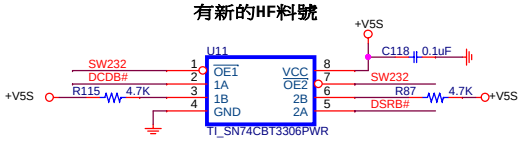




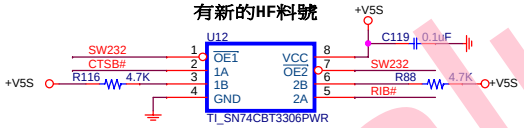
COM2



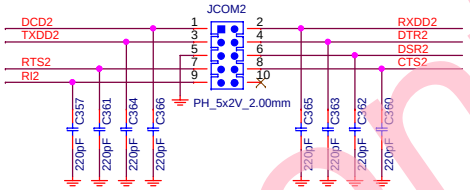
有新的HF料號



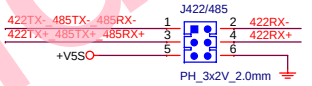
有新的HF料號



COM2 Connector

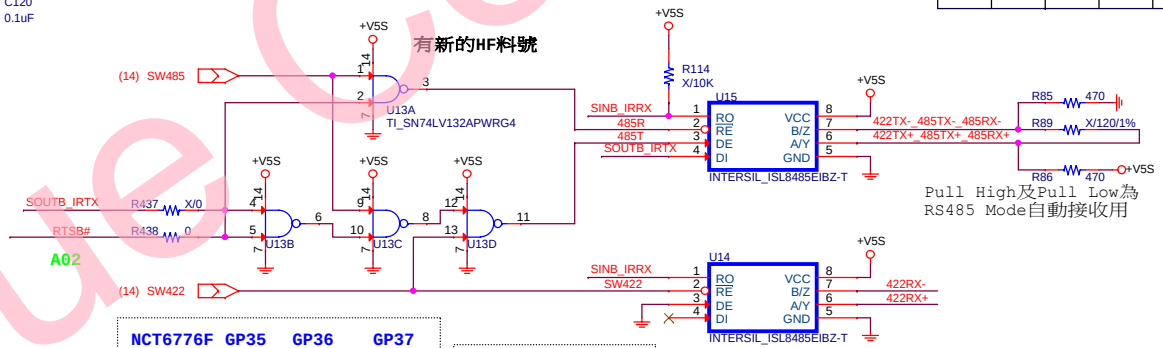


RS485/422 Connector



	PIN1	PIN2	PIN3	PIN4
RS422	TX-	RX-	TX+	RX+
RS485	TX-		TX+	

有新的HF料號



NCT6776F GP35 GP36 GP37

GPIO:	SW232	SW422	SW485
RS232:	<HI>	HI	LO
RS422:	LO	<LO>	LO
RS485:	LO	HI	<HI>
IR :	LO	HI	LO

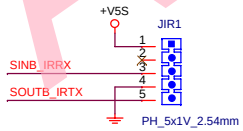
SN74LV132APWRG4

A	B	Y
H	H	L
L	X	H
X	L	H

RS485 Mode

SOUTB_IRTX	485R	485T
L	H	H
H	L	L

IR



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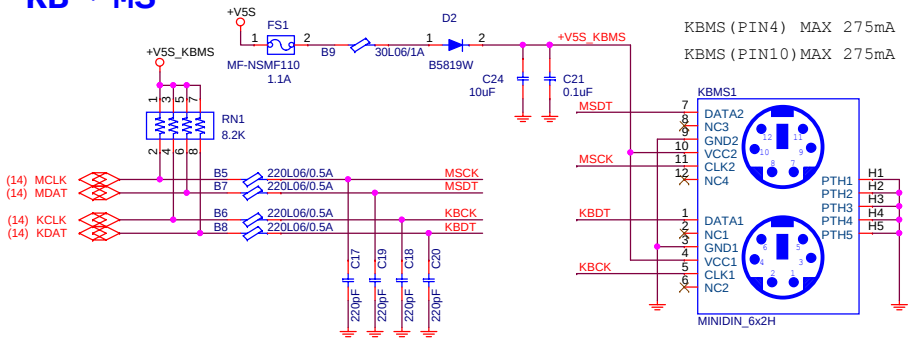
Project Name	Module Number	Rev
EEV-EX14	<Module no.>	?

Size	Title	Rev
A3	COM1、COM2	A2

Date: Wednesday, June 15, 2016 Sheet 15 of 23

KB、MS

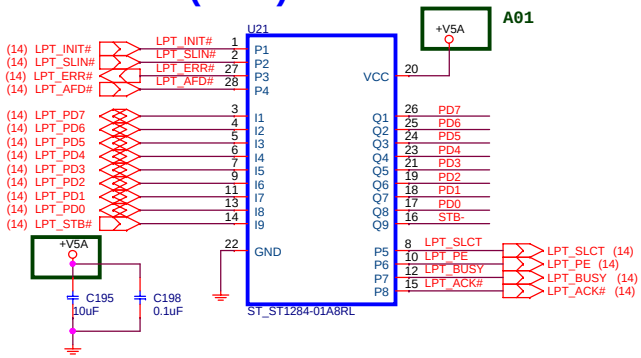


KB、MS Connector

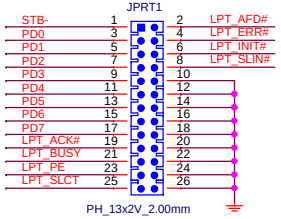
KBMS(PIN4) MAX 275mA

KBMS(PIN10)MAX 275mA

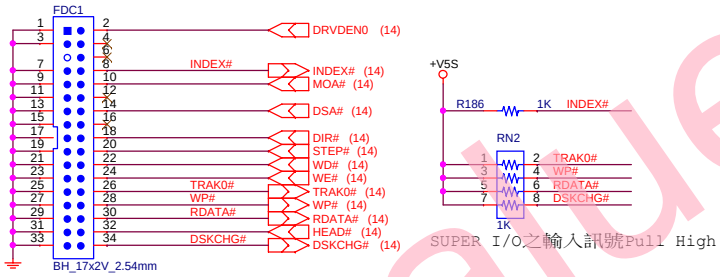
PRINTER(PRT)



PRINTER Connector

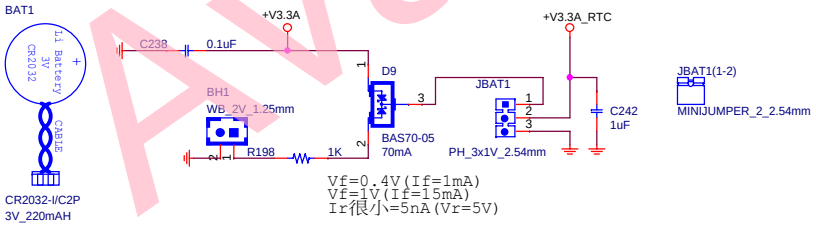


FLOPPY Connector(FDC)



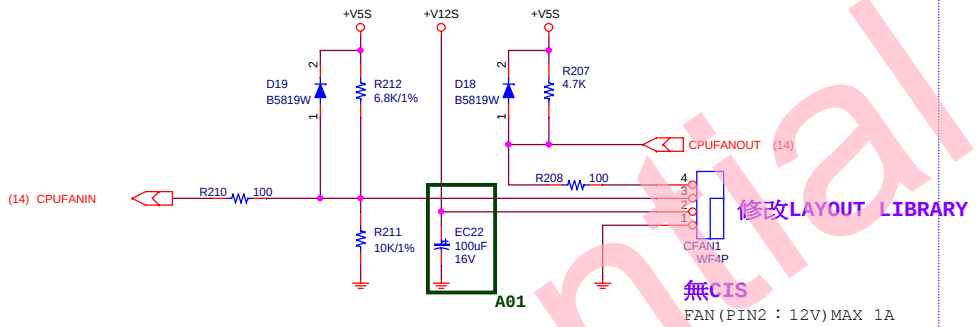
SUPER I/O之輸入訊號Pull High

BATTERY



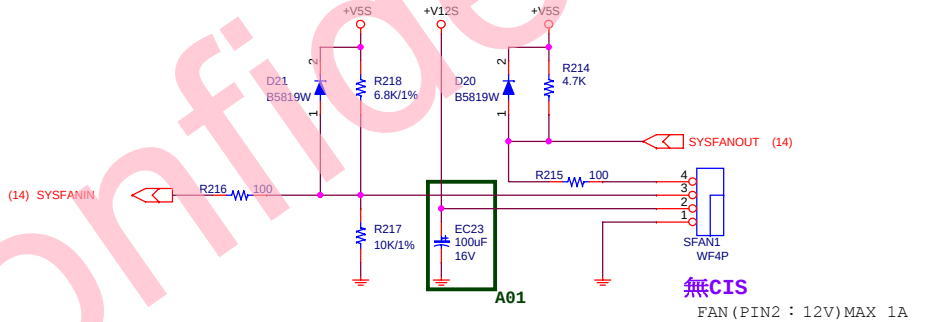
Vf=0.4V(If=1mA)
Vf=1V(If=15mA)
Ir很小=5nA(Vr=5V)

CPUFAN0

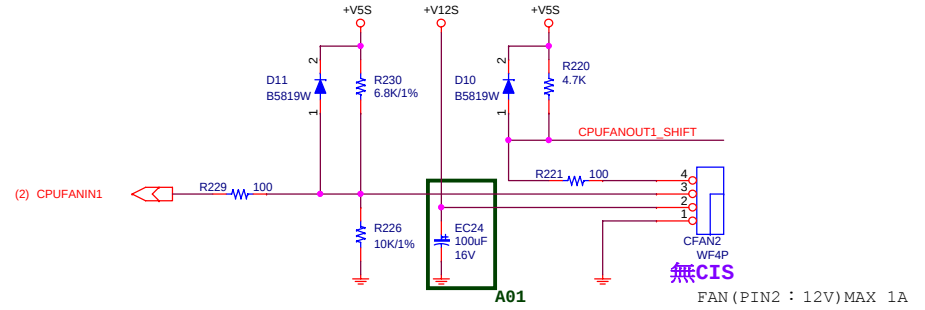


修改LAYOUT LIBRARY

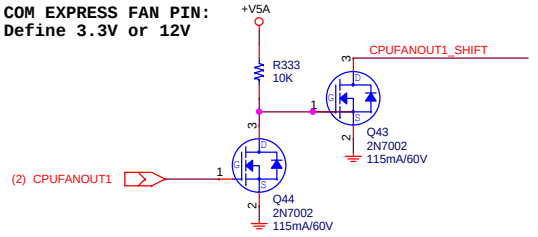
SYSFAN0



CPUFAN1



COM EXPRESS FAN PIN:
Define 3.3V or 12V



A01

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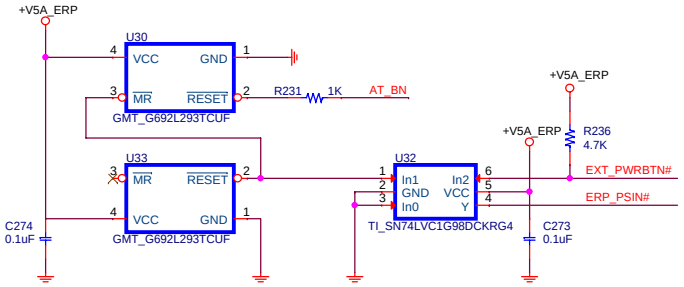
Project Name	Module Number	Rev
EEV-EX14	<Module no.>	?

Size	Title	Rev
A3	KB、MS、PRT、FDC、BAT、FAN	A2

Date: Wednesday, June 15, 2016 Sheet 16 of 23

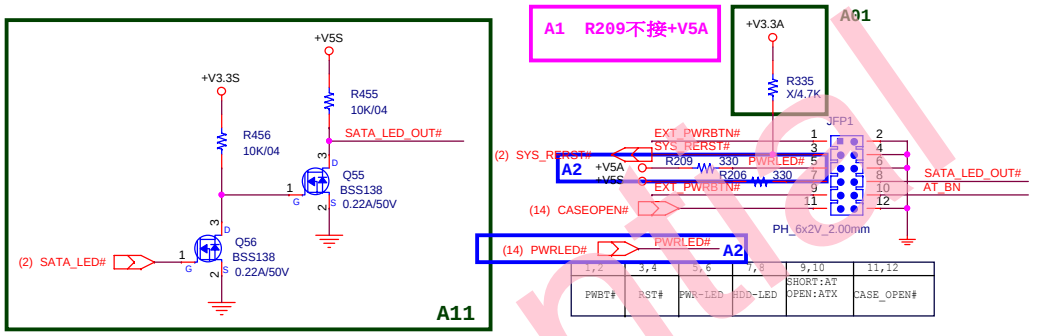
AUTO POWER ON



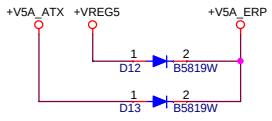
SN74LVC1G98

In2(6)	In1(1)	In0(3)	Y(4)
L	L	L	H
L	H	L	L
H	H	L	H
H	L	L	H

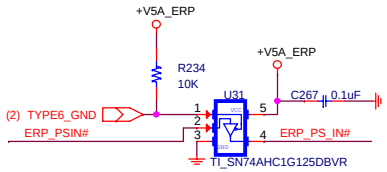
FRONT PANEL



因ErP有限制要低於0.5W
故需控制此3個電源的使用



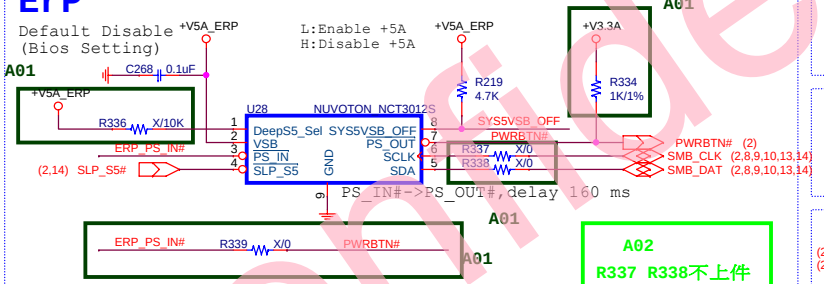
TYPE6_GND於上板接地



ErP

Default Disable
(Bios Setting)

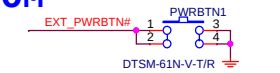
L:Enable +5A
H:Disable +5A



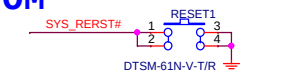
Add R336(10K上件) R337 R338(0R不上件) R339(0R上件),
可使下板ERP不受BIOS控制，且不進Deep_S5

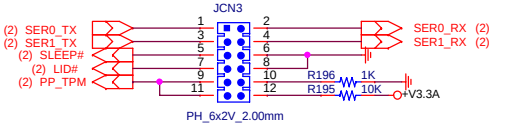
A02
R337 R338不上件

POWER BUTTOM

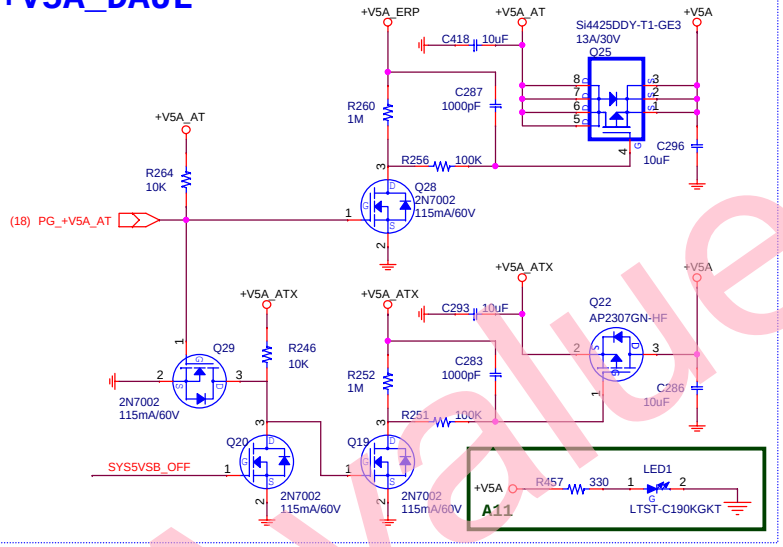


RESET BUTTOM

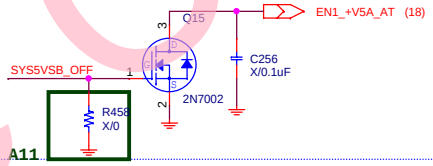




+V5A_DAUL



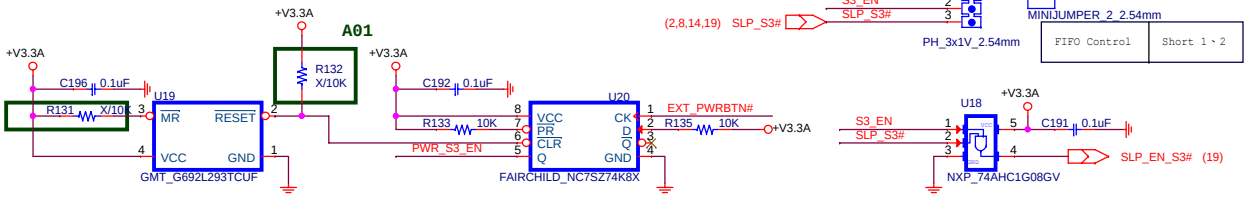
EN1:+V5A_AT



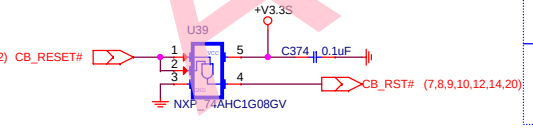
TPS51220A
EN1 EN2接地為DISABLE
EN1 EN2不接為ENABLE
電容落地為Soft Start

防止第一次開機S3為High而使電源轉出 --> JPWR1:Short 12
但若設定上板為AT開機時 --> JPWR1:Short 23
但若要使用ERP時 --> JPWR1:Short 23

防止第一次開機S3為High而使電源轉出



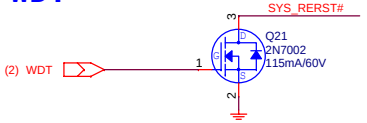
RESET BUFFER



SN74AHC1G08

A	B	Y
H	H	H
L	X	L
X	L	L

WDT



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Project Name	Module Number	Rev
EEV-EX14	<Module no.>	?

Size	Title	Rev
A3	V5A、ErP、FRONT	A2

Date: Wednesday, June 15, 2016 Sheet 17 of 23

DRVH1,DRVL1,DRVH2,DRVL2(PIN1,24,27,30)走20mils線寬
VREG3、VREG5、VREF2線寬拉10mils

TPS51220A SPEC INPUT 4.5V~32V
RMWxx0N03FUB Vds Max 30V
+VIN SPEC INPUT 9V~19V

+V3.3S轉出

Iout = 8A　無CIS　RDC=11mR　(output 100mA)　無CIS　Iout = 8A

+V5A_AT　+VIN　+VREG5　+V3.3S

U34 TI_TPS51220ARTVR　301.2KHz

Vout=(97.6K/23.7K)+1=5.12V

Vout=(54.9K/23.7K)+1=3.32V

EN2:+V3.3S

PGOOD2 +V3.3S

+V5S轉出

+V3.3A轉出

APW7145 SPEC INPUT 4.3V~14V
OUTPUT MAX 3A

Vout=0.8x(1+47.5K/15K)=3.33V MAX 3A

EN:0.5V~2.1V

SS time Setting EN1,2 pin cap	
X	Standard 0.96mS
2200pF	1.1mS
3600pF	1.8mS
5600pF	2.8mS
8200pF	4.1mS

t = C / ISS
ISS=2uA

t = 0.0022uF / 2uA
= 1.1mS

SKIPSEL(PIN6 19)	
GND	Continuous conduction mode
VREG2	Auto Skip
VREG3	Auto Skip,maximum 7 skip (suitable for FSW< 400KHz)
VREG5	Auto SKIP, maximum 15 skip (suitable for equal to or greater than 400KHz)

FUNC(PIN11)
GND: Current mode, OVP enable
VREF2: D-CAP mode, OVP disable
VREG3: D-CAP mode, OVP enable
VREG5: Current mode, OVP disable

Overcurrent trip level and discharge mode
TRIP (PIN14)
GND: V(OCL-ULV) , discharge on
VREF2: V(OCL-ULV), discharge off
VREG3: V(OCL-LV), discharge off
VREG5: V(OCL-LV), discharge on

$$I_{OCL(PEAK)} = V_{OCL} \times \frac{1}{Rs} \times \frac{Rx + Rc}{Rc}$$

OCP=31mV*(1/9mr)*((7.5KR+1.6KR)/1.6KR)=16A

+VIN -> VREG3 -> EN -> VREG5/VREF2 -> EN1/EN2 -> SW1/SW2 -> PG1/PG2

VREG5(PIN29)
當PGOOD1 High 時,
隔了7.7mS VREG5內部的LDO會被Shut Down,
改由V5SW供應5V電源.
PGOOD1 Low時,會改由內部LDO Output.

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Project Name	Module Number	Rev
EEV-EX14	PWR-04	A0

Size	Title	Rev
A3	V3.3A、V5S、V3.3S(TPS51220)	A2

Date: Wednesday, June 15, 2016　Sheet 18 of 23

LTC3780EG SPEC INPUT 4V~36V

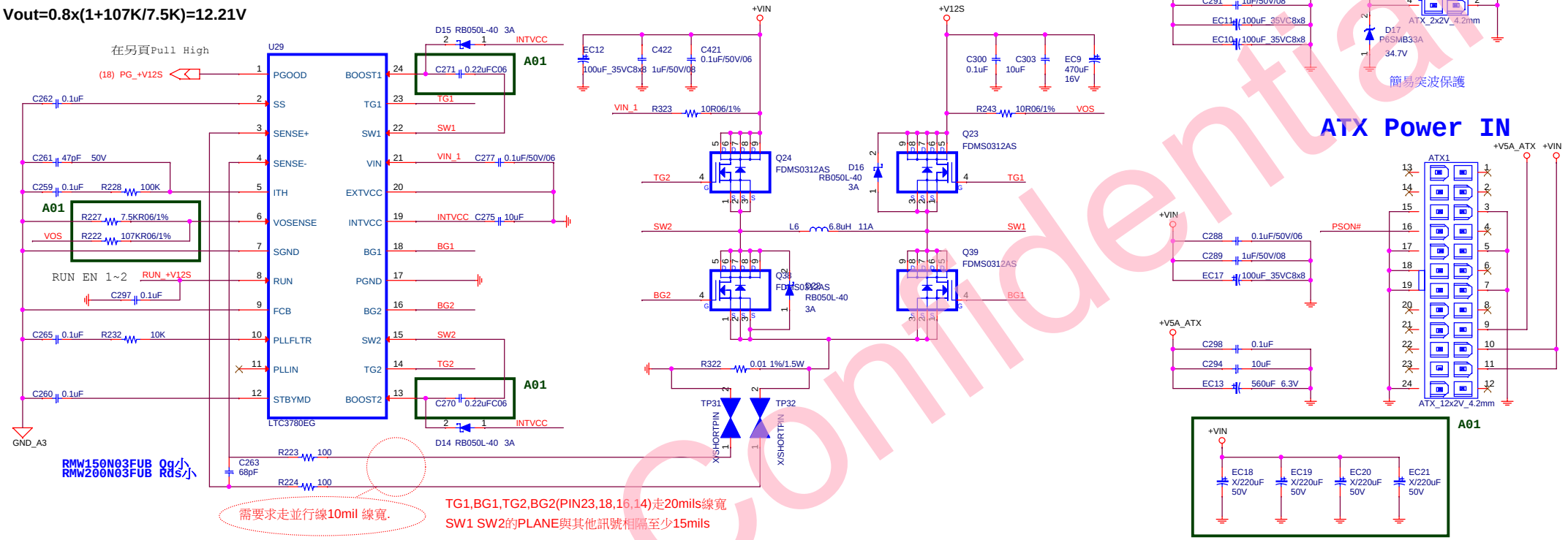
RMWxx0N03FUB Vds Max 30V

+VIN SPEC INPUT 9V~28V

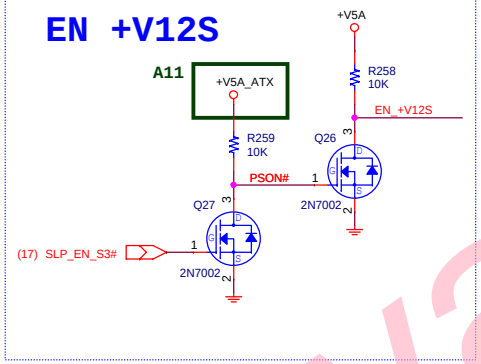
Vout=0.8x(1+107K/7.5K)=12.21V

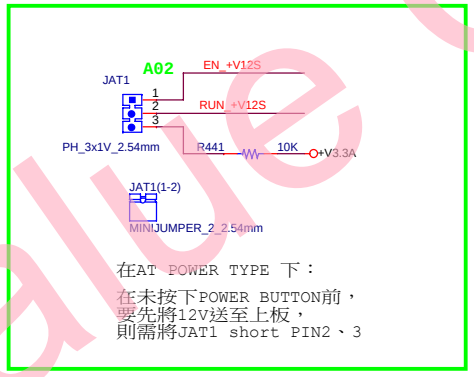
AT POWER IN

ATX Power IN



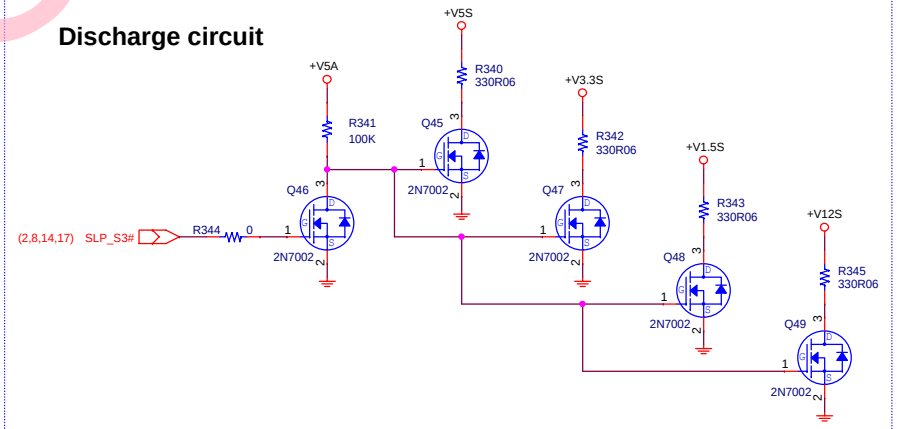
EN +V12S

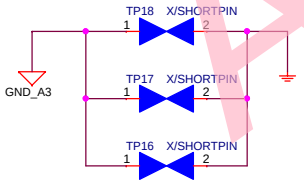




12V Control	Short 1、2
12V Always	Short 2、3

Discharge circuit





CHECK ITH及SENSE計算

VOSENSE-SET:
=VOS+*Rd/(Ru+Rd)
=12*2K/(28K+2K)
=0.8(為了發PGOOD)

PLLFLTR-SET:(INTVCC=6V)
0.1.2V --> 260KHz--330KHz
1.0.0V --> 170KHz--220KHz
2.2.4V --> 340KHz--440KHz

FCB:Forced Continuous Control Input(less than 0.8V)

PLLIN:External Synchronization Input to Phase Detector
STBYMD:LDO Control Pin

The BOOST1 pin swings from a diode voltage below INTVCC up to VOUT + INTVCC

The BOOST2 pin swings from a diode voltage below INTVCC up to VIN + INTVCC

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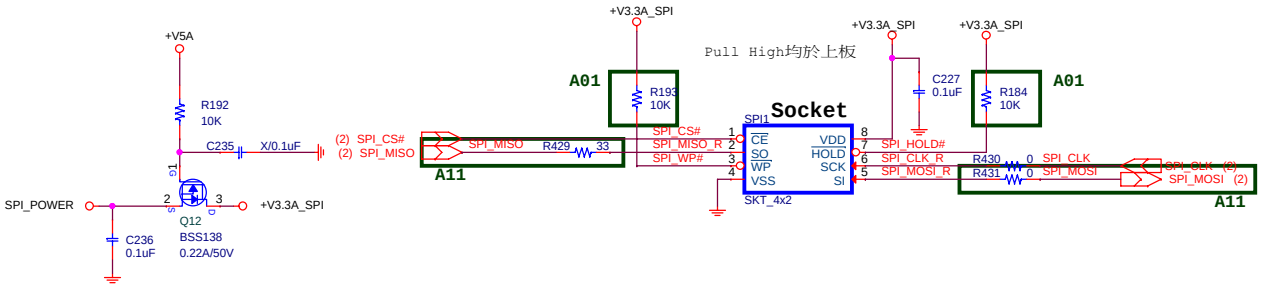
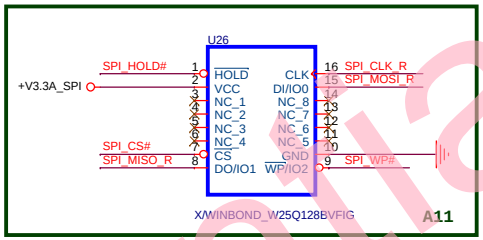
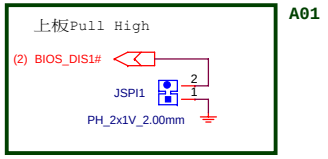
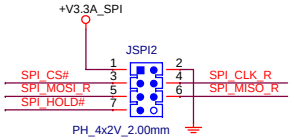
Project Name	EEV-EX14	Module Number	<Module no.> Rev ?
Size A3	Title	ATX & AT POWER(LTC3780:12V)	Rev A2
Date:	Wednesday, June 15, 2016	Sheet 19 of 23	

SPI BIOS







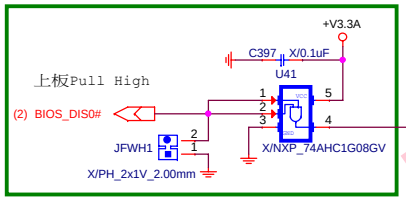


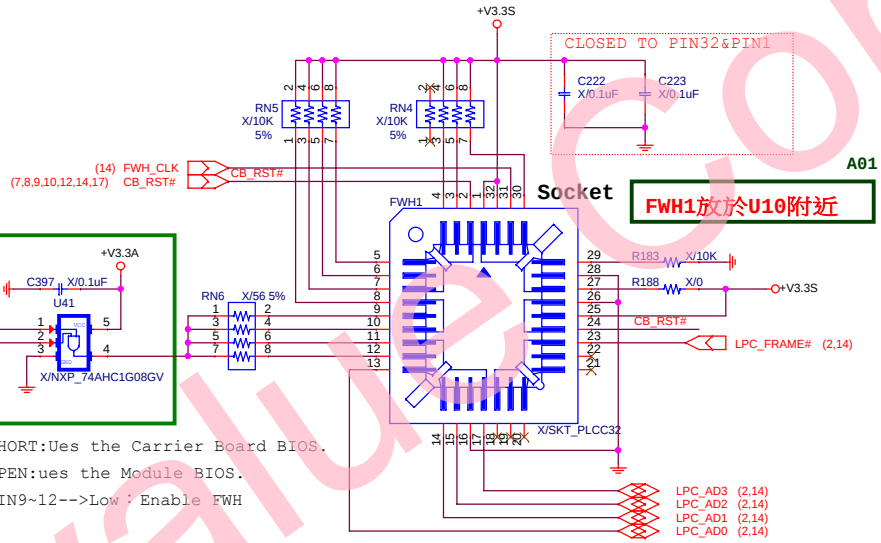
FWH BIOS

SN74AHC1G08

A	B	Y
H	H	H
L	X	L
X	L	L

A01-1





1G08:Iout Max:25mA
1G125:Iout Max:4mA

SHORT:Ues the Carrier Board BIOS.
OPEN:ues the Module BIOS.
PIN9~12-->Low : Enable FWH

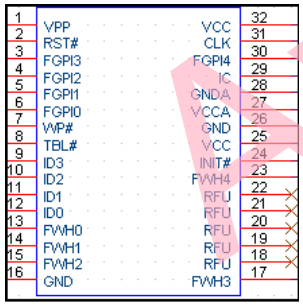
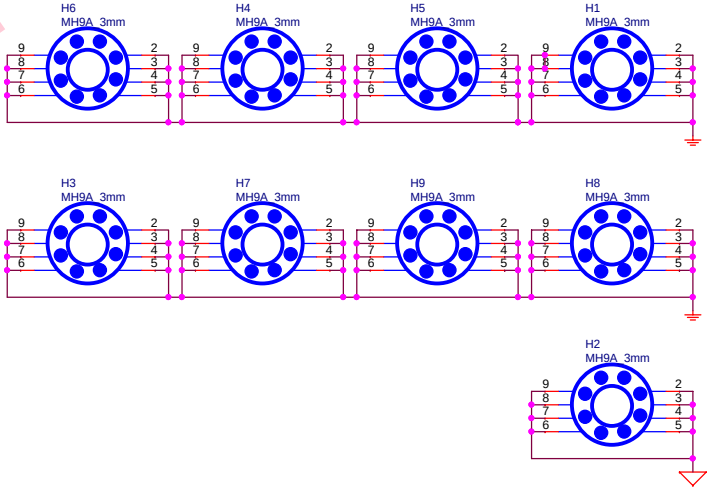


Table 4.13: Effect of the BIOS disable signals

BIOS_DIS1#	BIOS_DIS0#	Chipset SPI_CS1# Destination	Chipset SPI_CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	Ref Line
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	0	Module	Module	High	Module	Carrier FWH	1
0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	0	Carrier	Module	SPI1	Module	SPI0/SPI1	3



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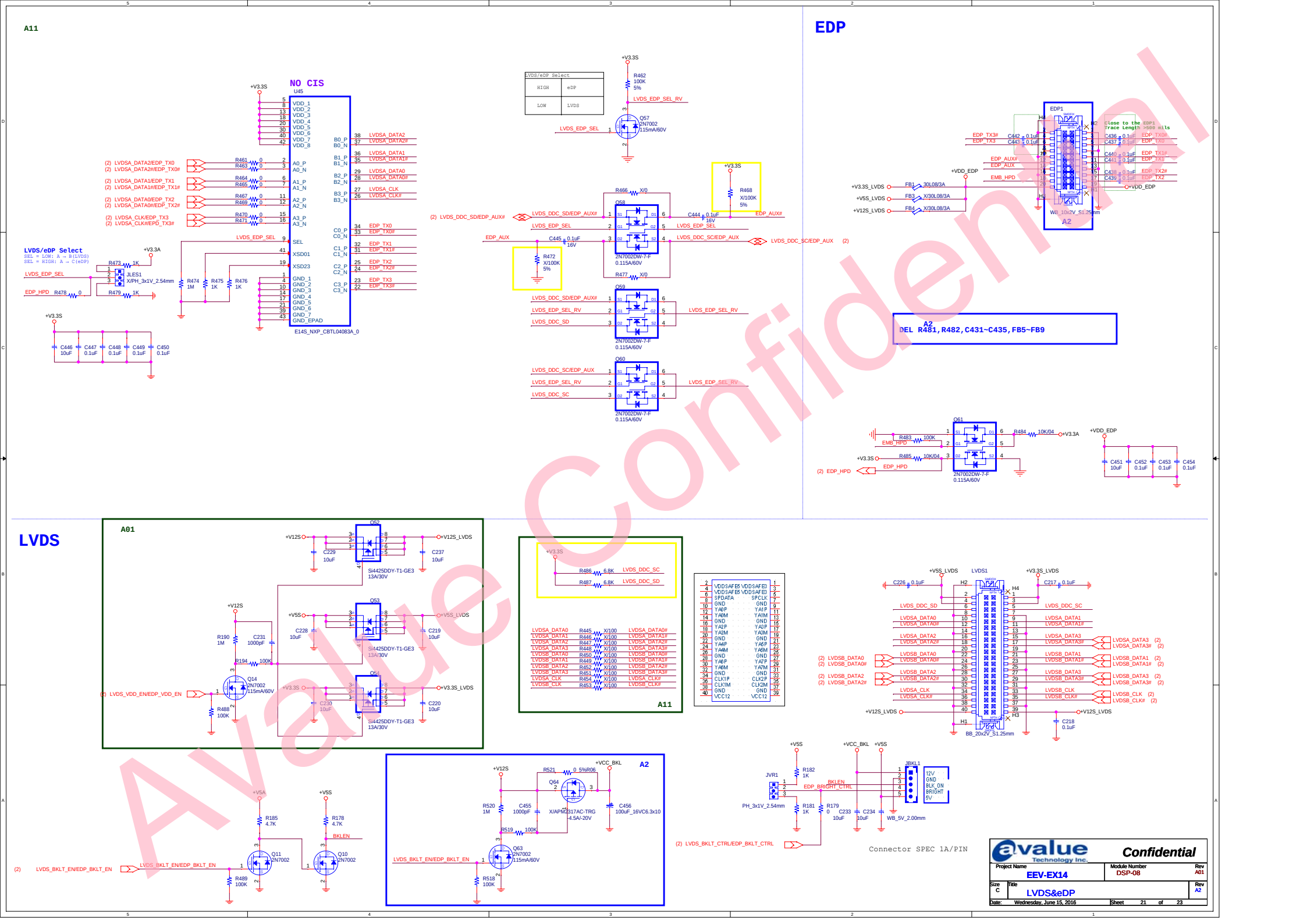
Project Name	Module Number	Rev
EEV-EX14	OTH-01	A0

Size	Title	Rev
A3	BIOS(SPI、FWH)	A2

Date: Wednesday, June 15, 2016 Sheet 20 of 23


A11
NO CIS
U45
E14S_NXP_CBTL04083A_0
LVDS/eDP Select
SEL = LOW: A → B(LVDS)
SEL = HIGH: A → C(eDP)
LVDS_EDP_SEL
EDP_HPD
JLES1
X/PH_3x1V_2.54mm
LVDS_EDP_SEL_RV
LVDS_DDC_SD/EDP_AUX#
EDP_AUX
2N7002DW-7-F
0.115A/60V
LVDS_DDC_SC/EDP_AUX
LVDS_DDC_SD
LVDS_DDC_SC
EDP
EDP1
BB_10x2V_S1.25mm
A2
DEL R481,R482,C431~C435,FB5~FB9
Close to the EDP1 Trace Length >500 mils
EDP_TX3#
EDP_TX3
EDP_AUX#
EDP_AUX
EMB_HPD
+VDD_EDP
+V3.3S_LVDS
+VSS_LVDS
+V12S_LVDS
30L08/3A
WB_10x2V_S1.25mm
LVDS
A01
Si4425DDY-T1-GE3
13A/30V
Q14
2N7002
115mA/60V
LVDS_VDD_EN/EDP_VDD_EN
+V12S_LVDS
+VSS_LVDS
+V3.3S_LVDS
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3
LVDSA_CLK
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3
LVDSB_CLK
X/100
A11
VDDSAFE5 VDDSAFE5
VDDSAFE5 VDDSAFE5
SPDATA SPCLK
GND GND
YA1P YA1P
YA0M YA1M
GND GND
YA2P YA2P
YA2M YA3M
GND GND
YA4P YA6P
YA4M YA6M
GND GND
YA6P YA7P
YA6M YA7M
GND GND
CLK1P CLK2P
CLK1M CLK2M
GND GND
VCC12 VCC12
BB_20x2V_S1.25mm
LVDSA_DATA3#
LVDSB_DATA3#
LVDSB_CLK#
A2
Q64
X/APM2317AC-TRG
-4.5A/-20V
Q63
2N7002
115mA/60V
LVDS_BKLT_EN/EDP_BKLT_EN
Q11
Q10
BKLEN
JVR1
JBKLT1
12V
GND
BLK_ON
BRIGHT
6V
PH_3x1V_2.54mm
WB_5V_2.00mm
LVDS_BKLT_CTRL/EDP_BKLT_CTRL
Connector SPEC 1A/PIN
Avalue Confidential
avalue Technology Inc.
Confidential
Project Name
EEV-EX14
Module Number
DSP-08
Rev
A01
Size
C
Title
LVDS&eDP
Rev
A2
Date:
Wednesday, June 15, 2016
Sheet
21
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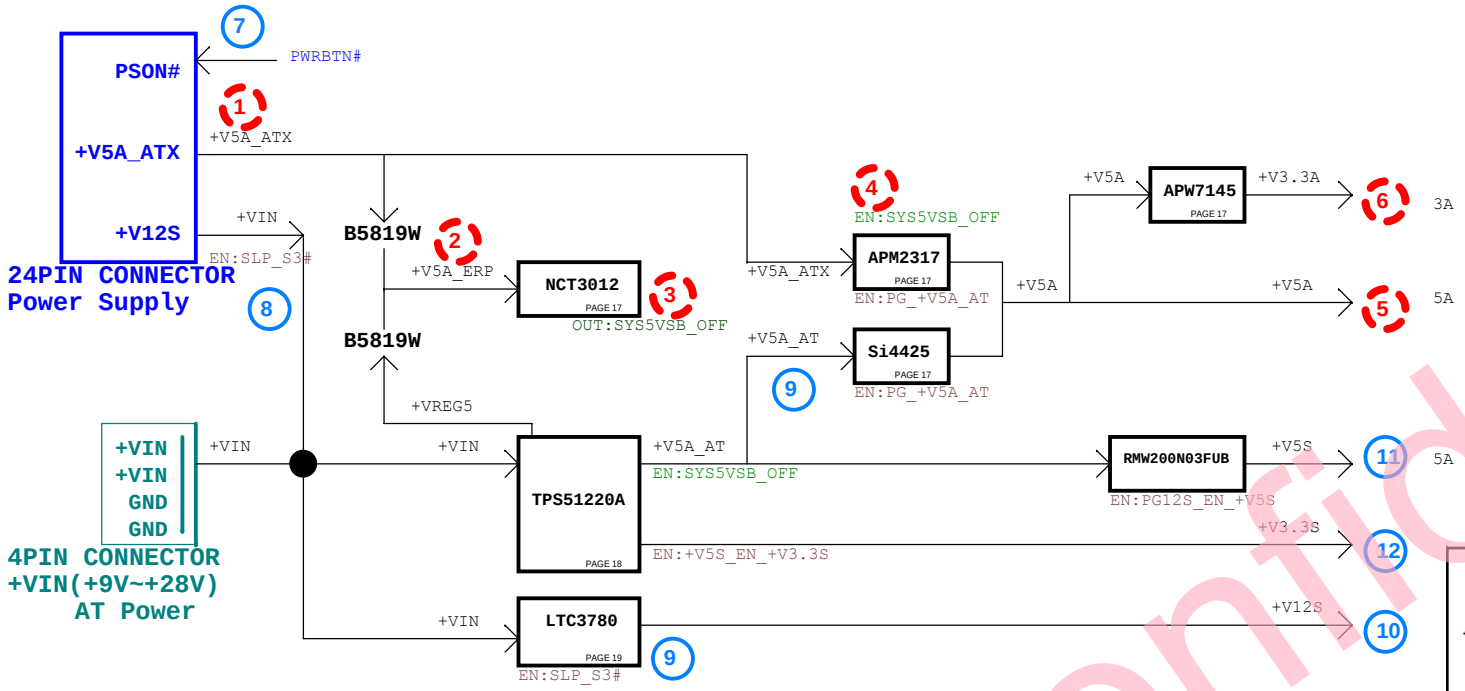
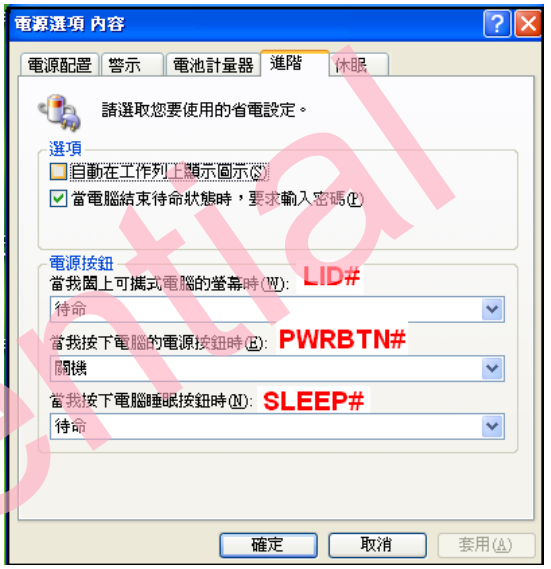
23





COM EXPRESS CONNECTOR

PIN(D57)	PIN(C57)	PIN(C54)	
TYPE2#	TYPE1#	TYPE0#	
X	X	X	Pin-out Type 1
NC	NC	NC	Pin-out Type 2
NC	NC	GND	Pin-out Type 3 (no IDE)
NC	GND	NC	Pin-out Type 4 (no PCI)
NC	GND	GND	Pin-out Type 5 (no IDE, no PCI)
GND	NC	NC	Pin-out Type 6 (no IDE, no PCI)

Module板 對 TYPE2# 接GND ~~ 以示爲TYPE 6 PIN DEFINE
Carrier板 用此PIN來控制12V的輸出

COM EXPRESS CONNECTOR

PIN(A97)

TYPE10#	
NC	Pin-out R2.0
PD	Pin-out Type 10 pull down to ground with 4.7K resistor
12V	Pin-out R1.0

NCT6776F
+V3.3A 0.008A
+V3.3S 0.025A

ALC892
+V5S 0.046A
+V3.3S 0.012A

RTL8111E
+V3.3A 0.070A+0.100A

ICS9DB633AFLF
+V3.3S 0.250A

ASM1440 X4
+V3.3S 0.005A*4

LAN2
+V3.3A 0.020A

EXPRESS CARD
+V3.3A 0.250A
+V3.3S 1.000A
+V1.5S 0.500A

MINI-PCIE Slot
+V3.3A 1.100A
+V1.5S 0.375A

USB X6
+V5A 4.6A

FAN X3
+V12S 3A

LVDS
+V12S 3A
+V5S 3A
+V3.3S 2A

PCIE X16
+V12S 5.5A
+V3.3S 3A
+V3.3A 0.375A

PCIE X4
+V12S 2.1A
+V3.3S 3A
+V3.3A 0.375A

PCIE X16(ADD)
+V12S 2.1A
+V3.3S 3A
+V3.3A 0.375A

PCIE X1
+V12S 2.1A
+V3.3S 3A
+V3.3A 0.375A

CH7308C
+V3.3S 0.1A
+V2.5S 0.2A

VGA HDMI KBMS COM2 FAN PRT FDC APW7145(1.5V/1A)
+V5S 2A

Power Rail	PCIe x1, x4 or x8 Connector	PCIe x16 Connector	ExpressCard Connector	PCIe Mini Card Connector
VCC_12V	2.1A @ 1000uF bulk	5.5A @ 2000uF bulk		
VCC_3V3	3.0A @ 1000uF bulk	3.0A @ 1000uF bulk	1.35A	1.0A
VCC_3V3_SB	375mA @ 150uF bulk	375mA @ 150uF bulk	275mA	330mA
VCC_1V5			750mA	500mA

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Project Name	Module Number	Rev
EEV-EX14	<Module no.>	?

Size	Title	Rev
A3	POWER DISTRIBUTION	A2

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MODIFY HISTORY

A0 -> A01

1.Page2：Add 4 PCS 0603 0R,預留將來上下板5VSB斷開用
2.Page2：Add 線路,上下板SM BUS隔離用
3.Page2：Add USB3.0 Connector端0R電阻(TX RX均要)
4.Page3：USB3.0之EMI Bead CK1 ~ CK8已有CIS
5.Page4：Add C424(1uF),前版線路漏劃
6.Page4：ALC892之BIT_CLK改放至CHIP端
7.Page7：Y1(25M)改小(3.2X2.5)
8.Page7：LAN1 LAN2 改料，改使用右側雙燈 左側單燈之Connector
9.Page8：SIM CARD PIN1和MIMI-PCIE1 PIN8直接接,不接至3.3A
10.Page8：MINI-PCIE1的 TX對和RX對 接反修正
11.Page8：U25的+V3.3S_EC和+V3.3A_EC接反修正
12.Page8：APW7145的EN PIN預留0.1uF
13.Page9：Add R328(0R)
14.Page11：HDMI DP之EMI BEAD換廠內料(CK15~CK22)
15.Page11：HDMI DP之HPD預留Pull High Pull Low電阻
16.Page11：R266 100K不上件,ASM144S HPD_SINK內部已Pull Down 200K
17.Page12：Add 2 PIN Header,以利插DP轉卡時,Jump不上件(斷開用)
18.Page13：Add SATA3 Connector端0R電阻(TX RX均要)
19.Page13：DIO Connector 電源由拉3.3A改3.3S，並Colay Fuse限流
20.Page14：OVT# Pull High由5V改接3.3V
21.Page14：R42(0R)上件，SIO 內部Device Wake Function
22.Page14：更新Temperature Sensing線路
23.Page14：Add U43(LPC CLOCK BUFFER)
24.Page16：U21(PRINTER ESD IC)電源由V5S改接V5A
25.Page16：Add EC22 EC23 EC24，FAN Connector 12V穩壓用
26.Page16：Add Q43 Q44 R333，將上板的3.3V FANOUT(PWM) Level Shift成5V
27.Page17：預留R335(SYS_RERST# Pull High)，但不先件，以防上板未Pull High
28.Page17：新增R334(1K-1%)，ERP偵測3.3A OK後,再Delay160ms發Low Pulse用
29.Page17：Add 預留R336(10K不上件) R337 R338(0R) R339(0R不上件),此狀態下板ERP仍受BIOS控制
R336(10K上件) R337 R338(0R不上件) R339(0R上件),此狀態下板ERP不受BIOS控制
30.Page17：R131 R132不需上件，因其不會影響Reset時序
31.Page18：R261(0R上件),3.3V POWER GOOD要接給上板
32.Page18：Q40修正其DS接反之線路
33.Page19：C270 C271由用錯料的2200pF改回正確的2200nF
34.Page19：R222 R227阻值調整,使輸出為12.21V(實測為12.09V，修改前為11.89V)
35.Page19：VIN預留4PCS 220uF/50V,以利高瓦特數上板使用，如ESM-QM77
36.Page20：刪除C239(0.1uF) U26(1G125),上件R193 R184(10K),SPI_CS#由上板做控制
37.Page21：LVDS POWER 改為各電源使用各自的SO8 MOS

A01-> A02

01.Page2：R361 R362改連接+V5S，
依COM SPEC --> AT時要供至上板的5VSB PIN，可改用5V或不接
02.Page2：CN1 A86、A87 保留PIN，用0R接KB_RST#、KB_A20GATE(Super IO)
03.Page2：SMB Level Shift IC Control Gate由接+V5S改+V3.3S
04.Page2：CN1 PIN D97(PEG_ENABLE#)接0R至地
05.Page2：CN1 PIN D54(PEG_LANE_RV#)預留接0R至地
06.Page7：LAN1 & LAN2 LED線路修正
07.Page8：SIM1 LAYOUT LIBRARY修正
08.Page8：EXPRESS1 & EXPRESS2 舊料停產，改料改LAYOUT
09.Page8：U25 PIN1 SYSRST#(本接EXCD0_PERST#) 留0R接CB_RST#
10.Page8：EXCD0_PERST# 改預留0R接至PERST#
11.Page15：RS485的控制(U13)預留原來的SOUTB_IRTX，改用RTSB#
12.Page19：新增JAT1 PIN HEADER
在AT POWER TYPE 下：在未按下POWER BUTTON前，
要先將12V送至上板，則需將JAT1 short
13.Page17：預設ErP不啟動(SMBUS 0R不上件) ~~ 由上板ErP運作

A02-> A1

01.Page03：USB3.0的串聯0R電阻去除
02.Page06：接至Device 的PCIE TX的0.1uF已加於Module Board，故此位置改上0R
03.Page17：Power LED本接+V5A，改+V5S
04.Page18：TPS51220的EN PIN線路修改(解決ATX POWER在S5時+VIN會有5V漏電)

A1-> A11

01.Page02：Modify CN1 Power in.
02.Page14：Add SIO I/O address jumper select
03.Page17：Modify SATA LED contorl.
04.Page19：Modify PSON# contorl.
05.Page20：Modify SPI connect.
06.Page21：Add LVDS/eDP switch & eDP connector

A11-> A2

01.Page2：Add R514
02.Page5：BOM Delete R287,R288
03.Page7：Add Q62,U46,R515,R516(op),R517
04.Page9：BOM Delete R162
05.Page10：Add U47,C457
06.Page11：Change U2 part number
07.Page14：Change U10,U43,R59,R60,R365,R281~R284 part number,Add Q65,RN7,RN8,delete R39,R306,BOM
Del R110,R118,R39
08.Page17：Change R209 net from +V5S to +V5A,Add net PWRLED#
09.Page21：Change EDP1 part number,Del R480~R482,C431~C435,FB5~FB9,Add Q63,Q64(op),R518~R521,C455,C456

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Project Name: EEV-EX14	Module Number: <Module no.>	Rev: ?
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